

COVER SHEET	1
BLOCK DIAGRAM	2
GPIO & JUMPER SETTING	3
Intel LGA775-CPU	4-6
nVidia - MCP73	7-15
DDR II DIMM 1and DIMM2 1 & 2	16-17
VGA & HDMI & DVI CONNECTOR	18
LAN - Realtek RTL8201CL	19
USB CONNECTORS	20
SIO-ITE 8718F	21
IDE & SATA& COM1& COM2& LPT	22
FAN & TPM	23
Azalia CODEC(ALC888S)	24
IEEE1394 VIA VT6308P	25
MS7 ACPI Controllor	26
FSB_VTT & NB_1P3V	27
VRM11 Intersil 6312 3Phase	28
PCI EXPRESS X16 & X 1 SLOT	29
PCI Slot 1 & 2	30
ATX & Front Panel	31
Audio De-Pop Circuit	32
Auto BOM manual	33
CLOCK DISTRIBUTION CHART	34
POWER DELIVERY CHART	35
POWER SEQUENCE	36

MS-7399

Version 2.0

CPU:

Intel Prescott (L2=2MB)
 Intel Cendar Mill (65nm)
 Intel Smithfield (90nm Dual core)
 Intel Presler (65nm Dual core)
 Intel Conroe (65nm Dual core)
 Intel Kentsfield
 Intel Yorkfield
 Intel Wolfdale

System Chipset:

nVidia - MCP73V

On Board Chipset:

BIOS -- SPI FLASH 4Mb
 Azalia CODEC(ALC 888S)
 LPC Super I/O -- ITE8718F
 LAN-Realtek RTL8201CL
 IEEE1394 -- VIA VT6308P

Main Memory:

DDR II * 2 (Max 2GB)

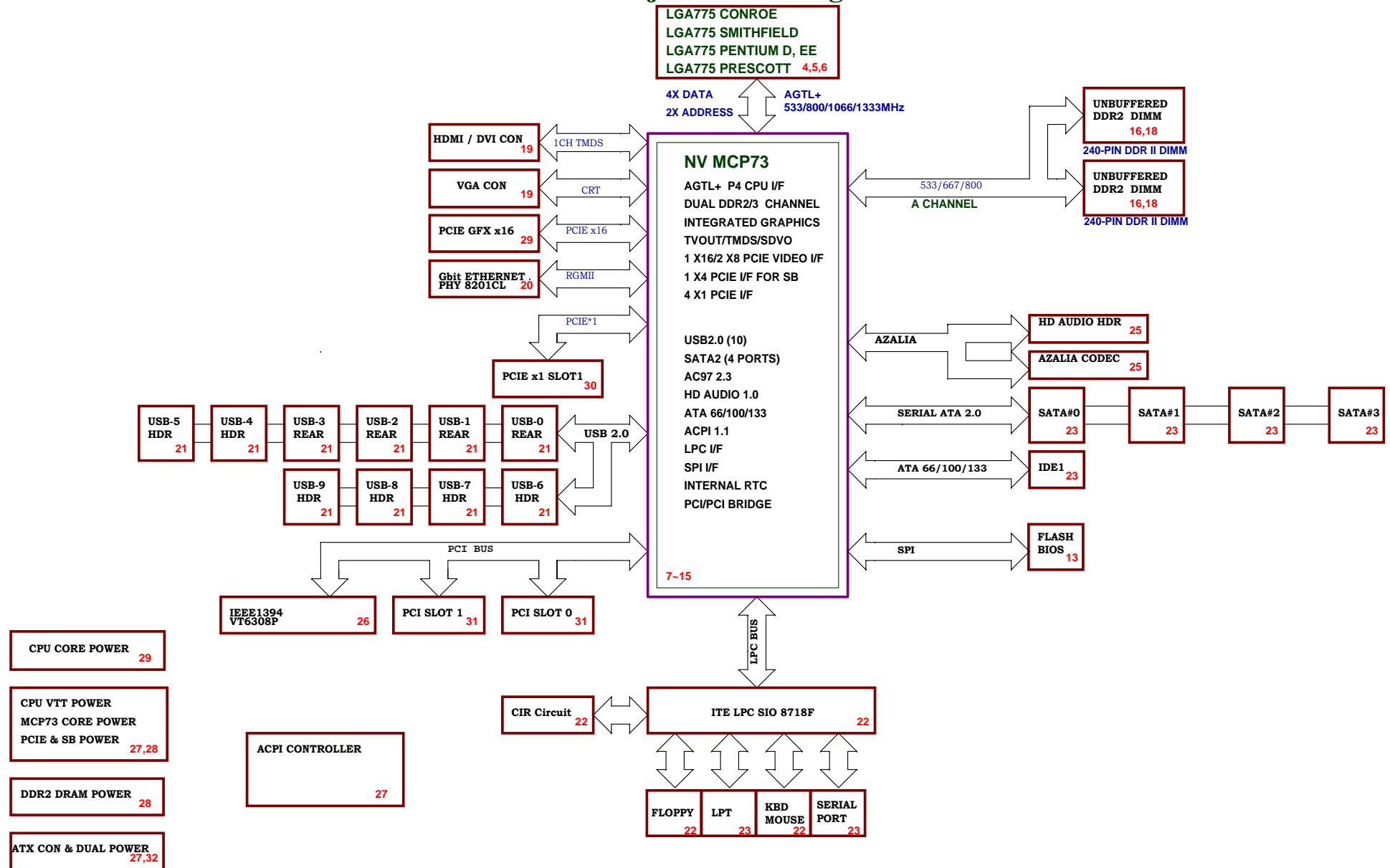
Expansion Slots:

PCI Express X16 SLOT * 1
 PCI Express X1 SLOT * 1
 PCI 2.3 SLOT * 2

Intersil PWM:

Controller: Intersil 6312 3 Phase

Project Block Diagram



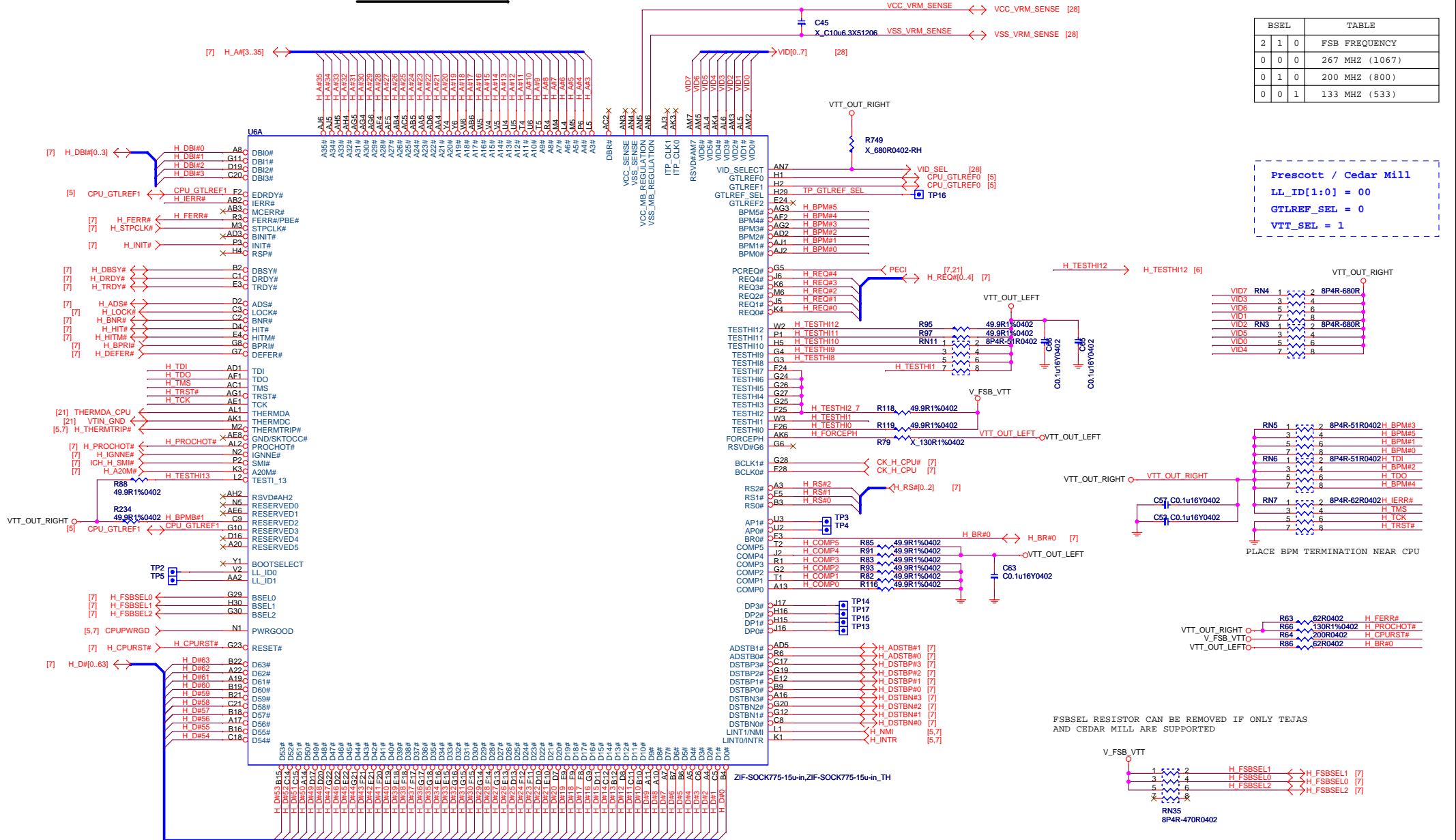
MCP73VE GPIO Config.

GPIO Pin	Type	Primary State
GPIO_2/NMI/PS2_CLK0	I/O(S5_3.3V)	Unused
GPIO_3/SMI#/PS2_DATA0	I/O(S5_3.3V)	Unused
GPIO_4/SCI/INTR/PS2_CLK1	I/O(S5_3.3V)	Unused
GPIO_5/INIT#/PS2_DATA1	I/O(S5_3.3V)	Unused
GPIO_6/FERR#/SYS_SERR#/IGPU_GPIO6	I/O(S5_3.3V)	Unused
GPIO_7/NFERR#/SYS_PERR#/IGPU_GPIO7	I/O(S5_3.3V)	Unused
GPIO_8/SPI_DI	I/O(S5_3.3V)	Unused
GPIO_9/SPI_DO	I/O(S5_3.3V)	Unused
GPIO_10/SPI_CS0	I/O(S5_3.3V)	Unused
GPIO_11/SPI_CLK	I/O(S5_3.3V)	Unused
LPC_DRQ1#/GPIO_19/FANRPM1	I/O(3.3V)	Unused
PROCHOT#/GPIO_20	I/O(CPU_VTT)	H_PROCHOT#
PE_WAKE#/GPIO_21	I/O(S5_3.3V)	WAKE#
HDA_SDATA_IN0/GPIO_22	I/O(S5_3.3V)	HDA_SDATA_IN
HDA_SDATA_IN1/GPIO_23/MGPIO_0	I/O(S5_3.3V)	Unused
HDA_SDATA_IN2/GPIO_24/MGPIO_2	I/O(3.3V)	Unused
USB_OC0#/GPIO_25	I/O(S5_3.3V)	OC#1
USB_OC1#/GPIO_26	I/O(S5_3.3V)	OC#2
USB_OC2#/GPIO_27	I/O(S5_3.3V)	OC#3
USB_OC3#/GPIO_28	I/O(S5_3.3V)	Pull Hi
USB_OC4#/GPIO_29	I/O(S5_3.3V)	Pull Hi
PCI_PME#/GPIO_30	I/O(S5_3.3V)	PCI_PME#
SIO_PME#/GPIO_31	I/O(S5_3.3V)	SIO_PME#
EXT_SMI#/GPIO_32	I/O(S5_3.3V)	LPC_SMI#
SUS_CLK/GPIO_34	I/O(S5_3.3V)	Unused
MII0_INTR/GPIO_35	I/O(S5_3.3V)	RGMI0_INTR#
MII0_PXER/GPIO_36/PWR_LED#	I/O(S5_3.3V)	RGMI0_RX_ER
MII0_PWRDWN/GPIO_37	I/O(S5_3.3V)	RGMI0_PREDN
PCI_REQ3#/GPIO_38/RS232_CTS#	I/O(3.3V)	PREQ#3
PCI_GNT3#/GPIO_39/RS232_RTS#	I/O(3.3V)	Unused
PCI_REQ2#/GPIO_40/RS232_DSR#	I/O(3.3V)	PREQ#2
PCI_GNT2#/GPIO_41/RS232_DTR#	I/O(3.3V)	PGNT#2
LPC_RESET#/GPIO_42	I/O(3.3V)	Unused
PCI_PERR#/GPIO_43/RS232_DCD#	I/O(3.3V)	PERR#
HDA_SYNC/GPIO_44	I/O(3.3V)	AZ_SYNC_R
HDA_SDATA_OUT/GPIO_45	I/O(3.3V)	HDA_SDATA_OUT
LPC_DRQ0#/GPIO_50	I/O(3.3V)	LPC_DRQ#0
PCI_REQ4#/GPIO52/RS232_SIN#	I/O(3.3V)	PREQ#4
PCI_GNT4#/GPIO_53/RS232_SOUT#	I/O(3.3V)	Unused
A20GATE/GPIO_55	I/O(3.3V)	A20GATE
KBRDRSTIN#/GPIO_56	I/O(3.3V)	KBRST#
SATA_LED#/GPIO_57	A(3.3V)	SATALED#
THERMTRIP#/GPIO_58	I/O(CPU_VTT)	H_THERMTRIP#
THERM#/GPIO_59	I/O(3.3V)	Unused
FANRPM0/GPIO_60	I/O(3.3V)	Unused
FANCTL0/GPIO_61	I/O(3.3V)	AUDIO_FRONT_IO
FANCTL1/GPIO_62	I/O(3.3V)	Unused
CABLE_DET_P/GPIO_63	I/O(3.3V)	ATADETO

PCI Config.

DEVICE	MCP1 INTX Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTX# PCI_INTY# PCI_INTZ# PCI_INTW#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTY# PCI_INTZ# PCI_INTW# PCI_INTX#	PREQ#1 PGNT#1	AD22	PCICLK1
1394	PCI_INTW#	PREQ#2 PGNT#2	AD23	1394_PCLK

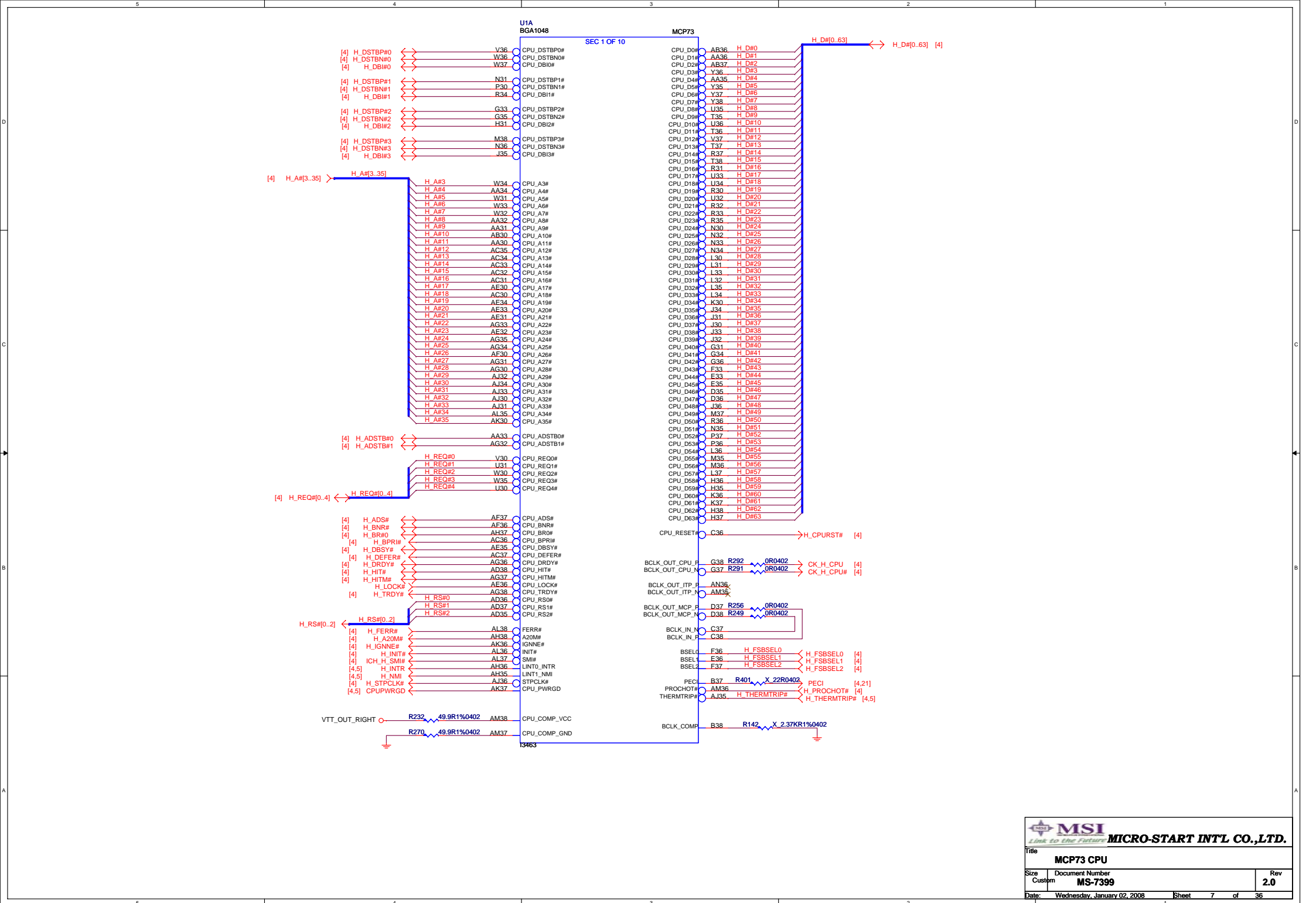
CPU SIGNAL BLOCK

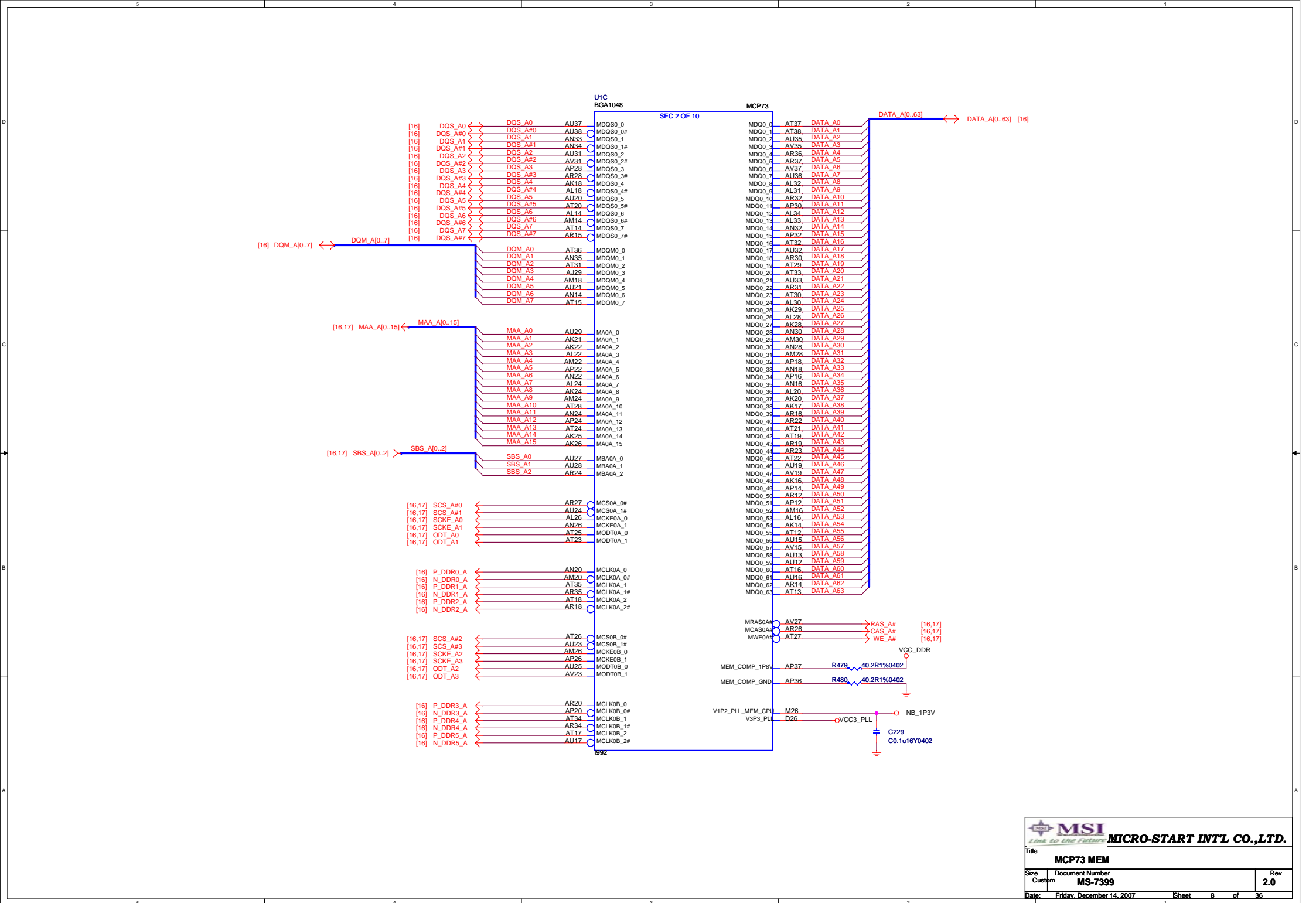


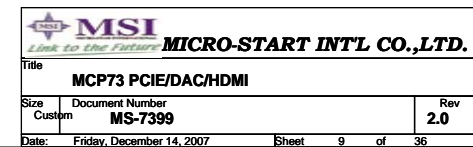
BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	267 MHZ (1067)
0 1 0	200 MHZ (800)
0 0 1	133 MHZ (533)

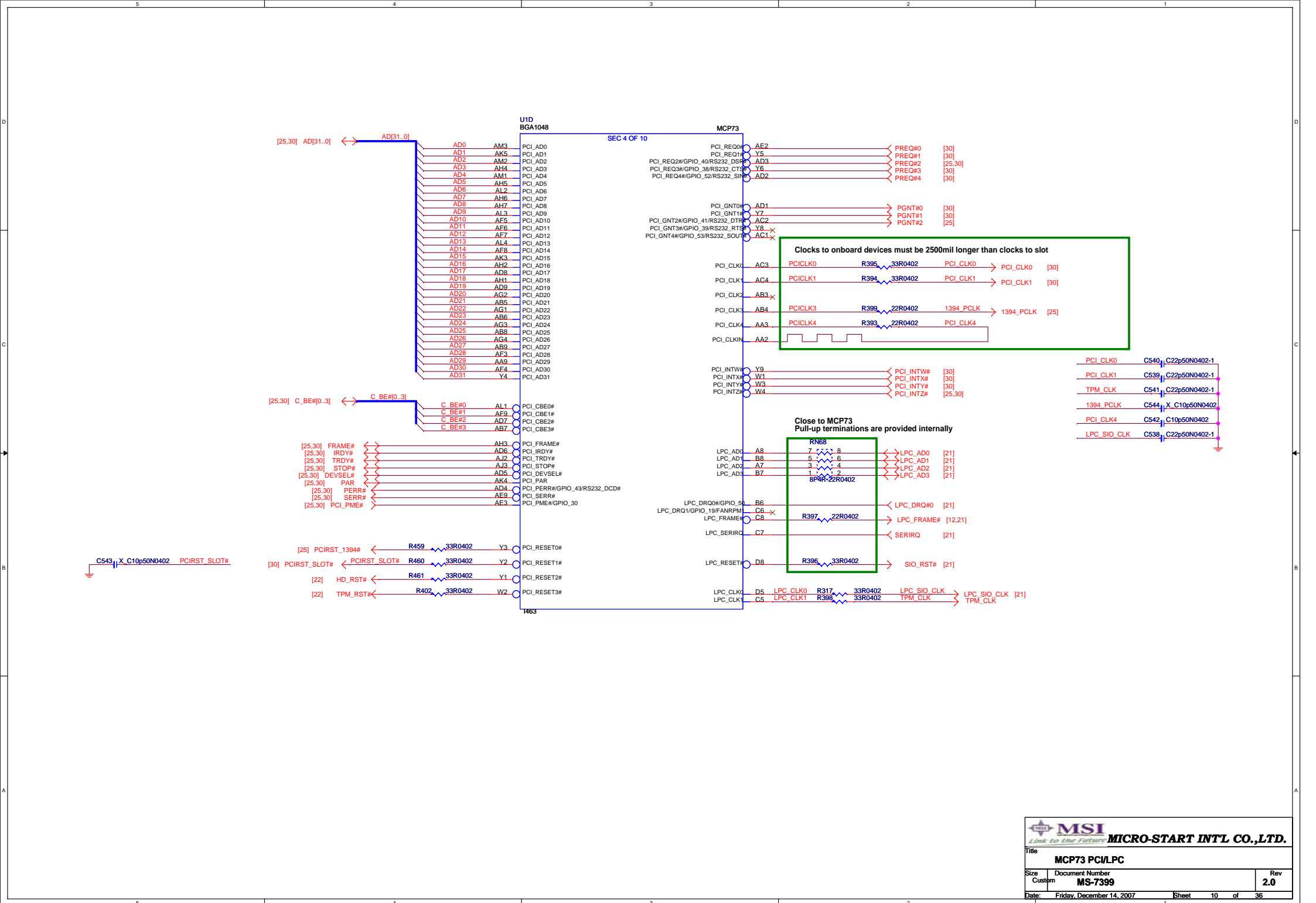
Prescott / Cedar Mill
 LL_ID[1:0] = 00
 GTLREF_SEL = 0
 VTT_SEL = 1

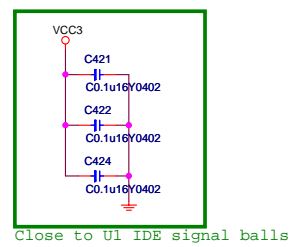
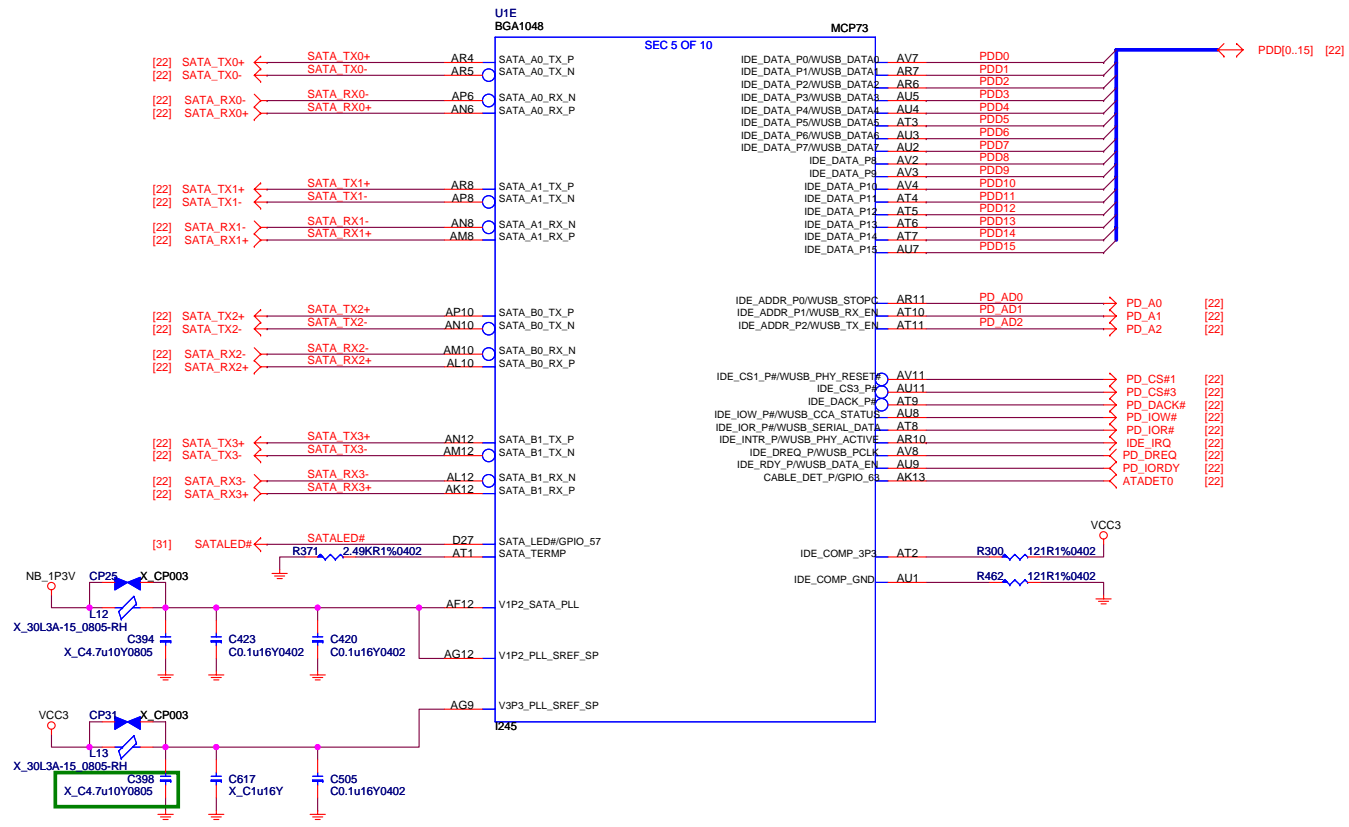
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED



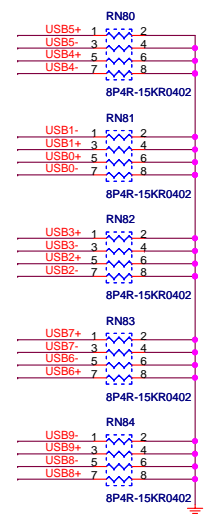
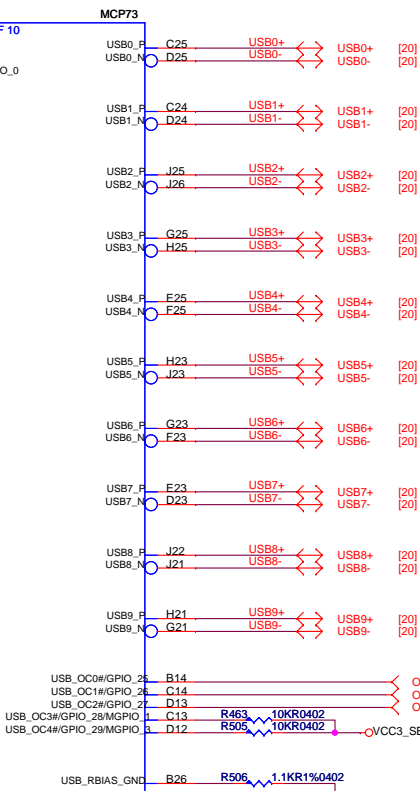
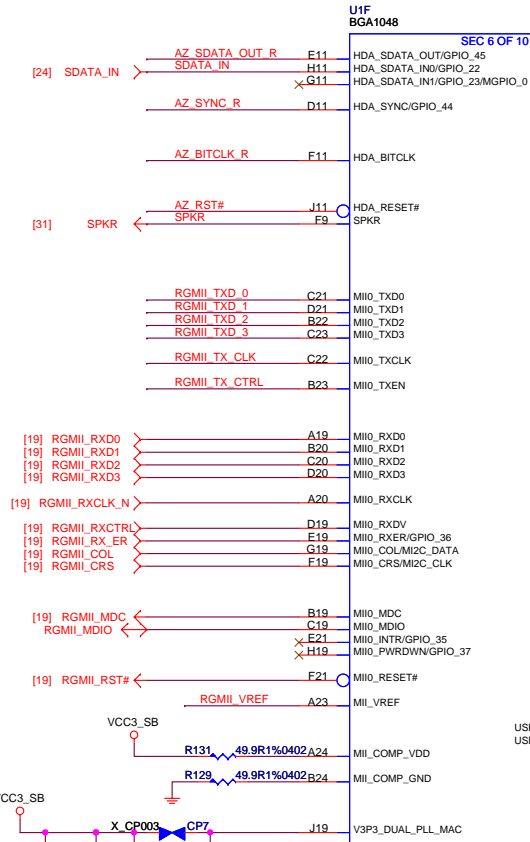
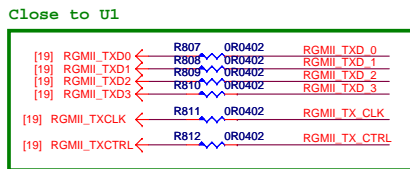
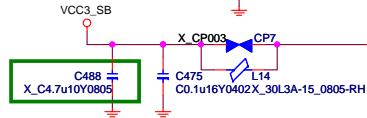
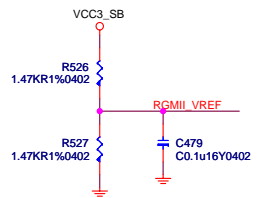
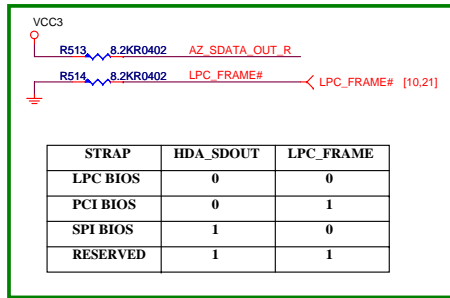
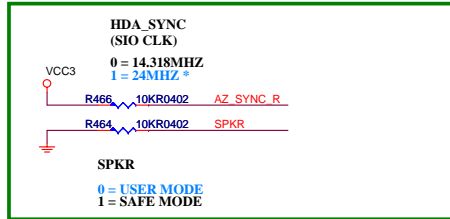
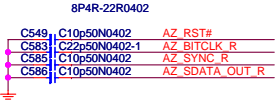
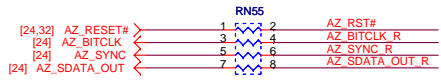
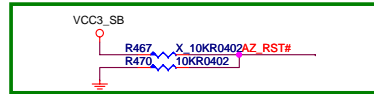


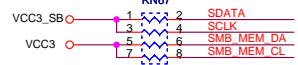
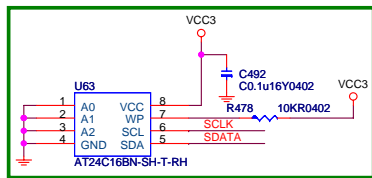




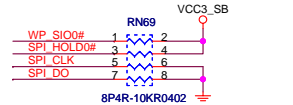
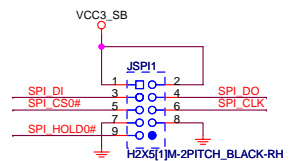
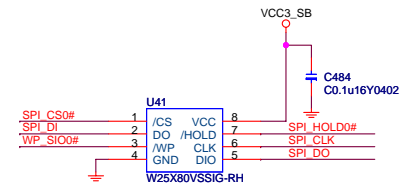
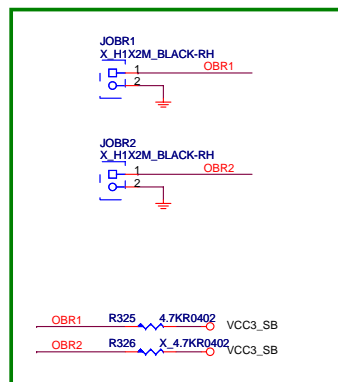
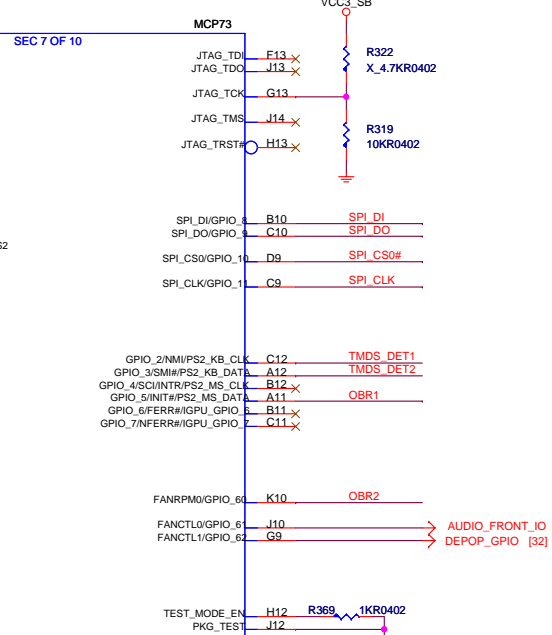
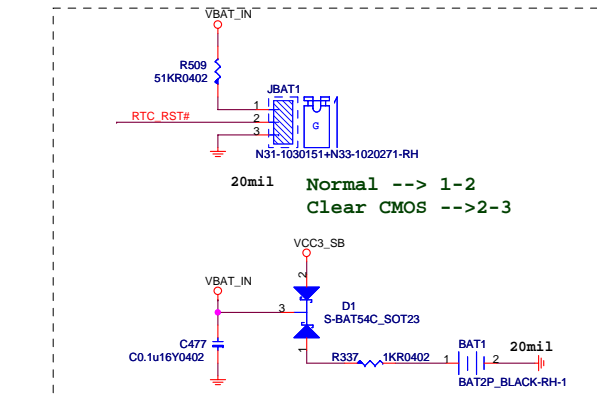
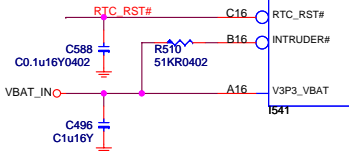
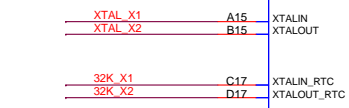
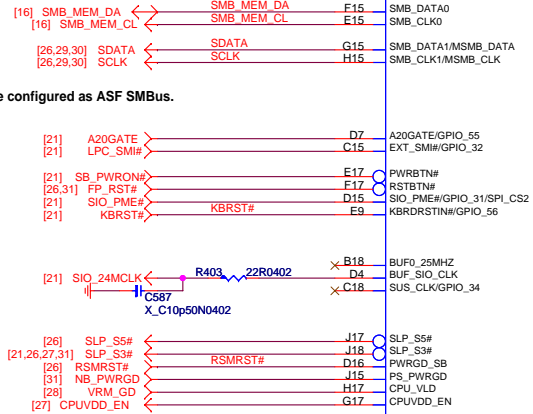
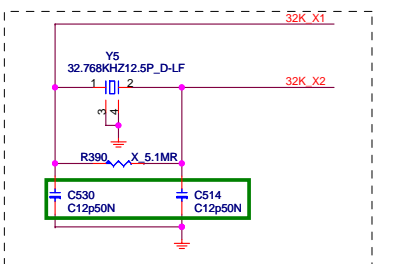
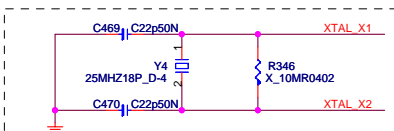
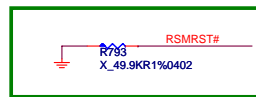
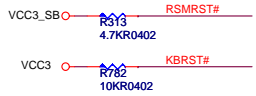


Strapping 10K ohm to VCC3_SB: RGMII
10K ohm to GND: MII



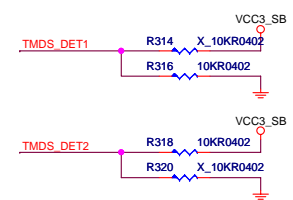


When SDATA/SCLK are not used, it can be configured as ASF SMBus.



MCP73 SPI CLK STRAP

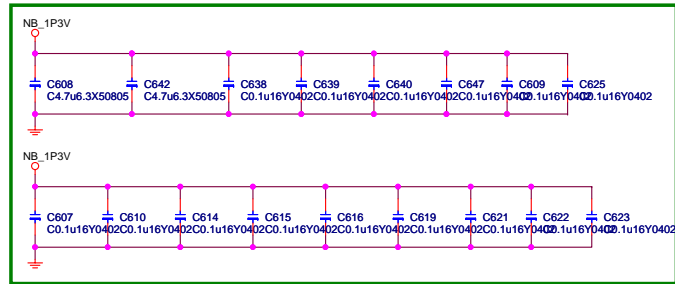
STRAP	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1



HDMI/DVI Detect

	TMDs_DET1	TMDs_DET2
DVI	1	0
HDMI	0	1
N/A	0	0

Bottom side



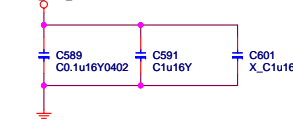
NB_1P3V	U11 BGA1048
AA12	VIP2_VDD_CORE
AA13	VIP2_VDD_CORE
AA19	VIP2_VDD_CORE
AA21	VIP2_VDD_CORE
AA22	VIP2_VDD_CORE
AA23	VIP2_VDD_CORE
AA24	VIP2_VDD_CORE
AA26	VIP2_VDD_CORE
AB12	VIP2_VDD_CORE
AB13	VIP2_VDD_CORE
AB15	VIP2_VDD_CORE
AB16	VIP2_VDD_CORE
AB17	VIP2_VDD_CORE
AB19	VIP2_VDD_CORE
AB21	VIP2_VDD_CORE
AB26	VIP2_VDD_CORE
AC12	VIP2_VDD_CORE
AC13	VIP2_VDD_CORE
AC17	VIP2_VDD_CORE
AC19	VIP2_VDD_CORE
AC21	VIP2_VDD_CORE
AC23	VIP2_VDD_CORE
AC24	VIP2_VDD_CORE
AC26	VIP2_VDD_CORE
AD12	VIP2_VDD_CORE
AD13	VIP2_VDD_CORE
AD17	VIP2_VDD_CORE
AD19	VIP2_VDD_CORE
AD21	VIP2_VDD_CORE
AD23	VIP2_VDD_CORE
AD26	VIP2_VDD_CORE
AE12	VIP2_VDD_CORE
AE26	VIP2_VDD_CORE
AH8	VIP2_VDD_CORE
AH9	VIP2_VDD_CORE
AJ10	VIP2_VDD_CORE
AJ6	VIP2_VDD_CORE
AJ8	VIP2_VDD_CORE
AJ9	VIP2_VDD_CORE
AK10	VIP2_VDD_CORE
AK6	VIP2_VDD_CORE
AK7	VIP2_VDD_CORE
AK8	VIP2_VDD_CORE
AK9	VIP2_VDD_CORE
AL6	VIP2_VDD_CORE
AL8	VIP2_VDD_CORE
AM4	VIP2_VDD_CORE
AM5	VIP2_VDD_CORE
AM6	VIP2_VDD_CORE
AN2	VIP2_VDD_CORE
AN3	VIP2_VDD_CORE
AN4	VIP2_VDD_CORE
AP3	VIP2_VDD_CORE
AP4	VIP2_VDD_CORE
AR1	VIP2_VDD_CORE
AR2	VIP2_VDD_CORE
AR3	VIP2_VDD_CORE
M23	VIP2_VDD_CORE
M24	VIP2_VDD_CORE
M25	VIP2_VDD_CORE
N23	VIP2_VDD_CORE
N24	VIP2_VDD_CORE
N25	VIP2_VDD_CORE
N26	VIP2_VDD_CORE
P26	VIP2_VDD_CORE
R18	VIP2_VDD_CORE
R20	VIP2_VDD_CORE
R22	VIP2_VDD_CORE
R24	VIP2_VDD_CORE
R26	VIP2_VDD_CORE
T18	VIP2_VDD_CORE
T20	VIP2_VDD_CORE
T22	VIP2_VDD_CORE
T26	VIP2_VDD_CORE
U18	VIP2_VDD_CORE
U20	VIP2_VDD_CORE
U22	VIP2_VDD_CORE
U23	VIP2_VDD_CORE
U24	VIP2_VDD_CORE
U26	VIP2_VDD_CORE
V15	VIP2_VDD_CORE
V16	VIP2_VDD_CORE
V17	VIP2_VDD_CORE
V18	VIP2_VDD_CORE
V20	VIP2_VDD_CORE
V26	VIP2_VDD_CORE
W20	VIP2_VDD_CORE
W21	VIP2_VDD_CORE
W22	VIP2_VDD_CORE
W23	VIP2_VDD_CORE
W24	VIP2_VDD_CORE
W26	VIP2_VDD_CORE
Y12	VIP2_VDD_CORE
Y13	VIP2_VDD_CORE
Y15	VIP2_VDD_CORE
Y16	VIP2_VDD_CORE
Y17	VIP2_VDD_CORE
Y18	VIP2_VDD_CORE
Y19	VIP2_VDD_CORE
Y26	VIP2_VDD_CORE

SEC 8 OF 10

MCP73
VIP2_CPU_VTT_A31
VIP2_CPU_VTT_A32
VIP2_CPU_VTT_AB27
VIP2_CPU_VTT_AD27
VIP2_CPU_VTT_B31
VIP2_CPU_VTT_B32
VIP2_CPU_VTT_C31
VIP2_CPU_VTT_C32
VIP2_CPU_VTT_C33
VIP2_CPU_VTT_D31
VIP2_CPU_VTT_D32
VIP2_CPU_VTT_D33
VIP2_CPU_VTT_E31
VIP2_CPU_VTT_F29
VIP2_CPU_VTT_F30
VIP2_CPU_VTT_F31
VIP2_CPU_VTT_G29
VIP2_CPU_VTT_H27
VIP2_CPU_VTT_H28
VIP2_CPU_VTT_H29
VIP2_CPU_VTT_J27
VIP2_CPU_VTT_J28
VIP2_CPU_VTT_J29
VIP2_CPU_VTT_K29
VIP2_CPU_VTT_M27
VIP2_CPU_VTT_N27
VIP2_CPU_VTT_P27
VIP2_CPU_VTT_T27
VIP2_CPU_VTT_V27
VIP2_CPU_VTT_Y27

V_FSB_VTT

V_FSB_VTT



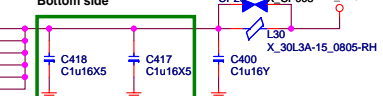
NB_1P3V
VIP2_PEX_DVDD_N13
VIP2_PEX_DVDD_R15
VIP2_PEX_DVDD_R16
VIP2_PEX_DVDD_T15
VIP2_PEX_DVDD_T16

VIP2_PEX_AVDD
N12
P12
P13
T12
T13
U12
U13
W12
W13

NB_1P3V
VIP2_SATA_DVDD_AD15
VIP2_SATA_DVDD_AE15
VIP2_SATA_DVDD_AE16
VIP2_SATA_DVDD_AG16

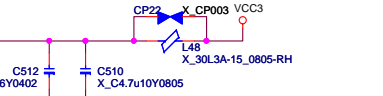
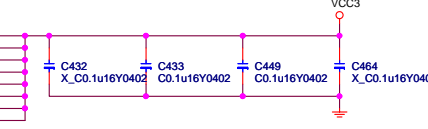
Bottom side

VIP2_SATA_AVDD
AE13
AE13
AE14
AG13
AG14
AG15



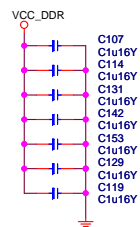
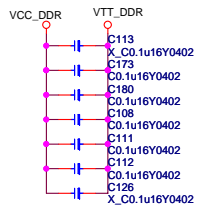
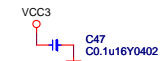
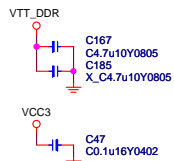
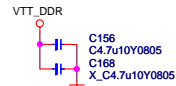
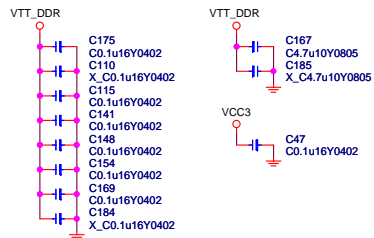
V3P3
AC6
AC8
AC9
AG6
AG8
W6
W8
W9

V3P3_DAC
F28

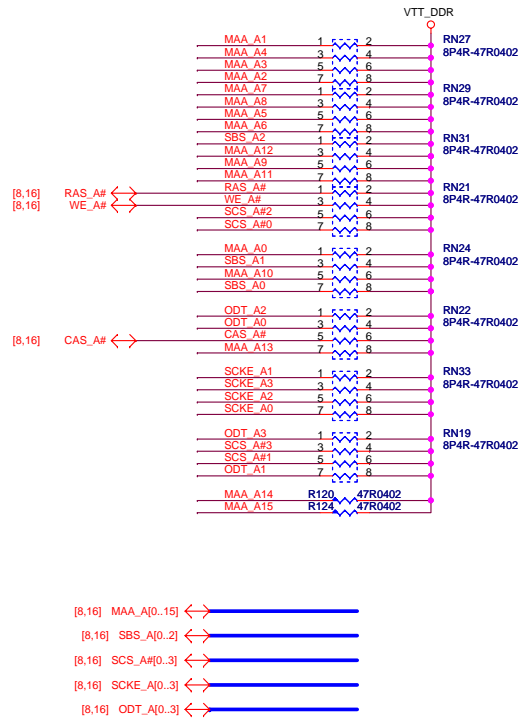


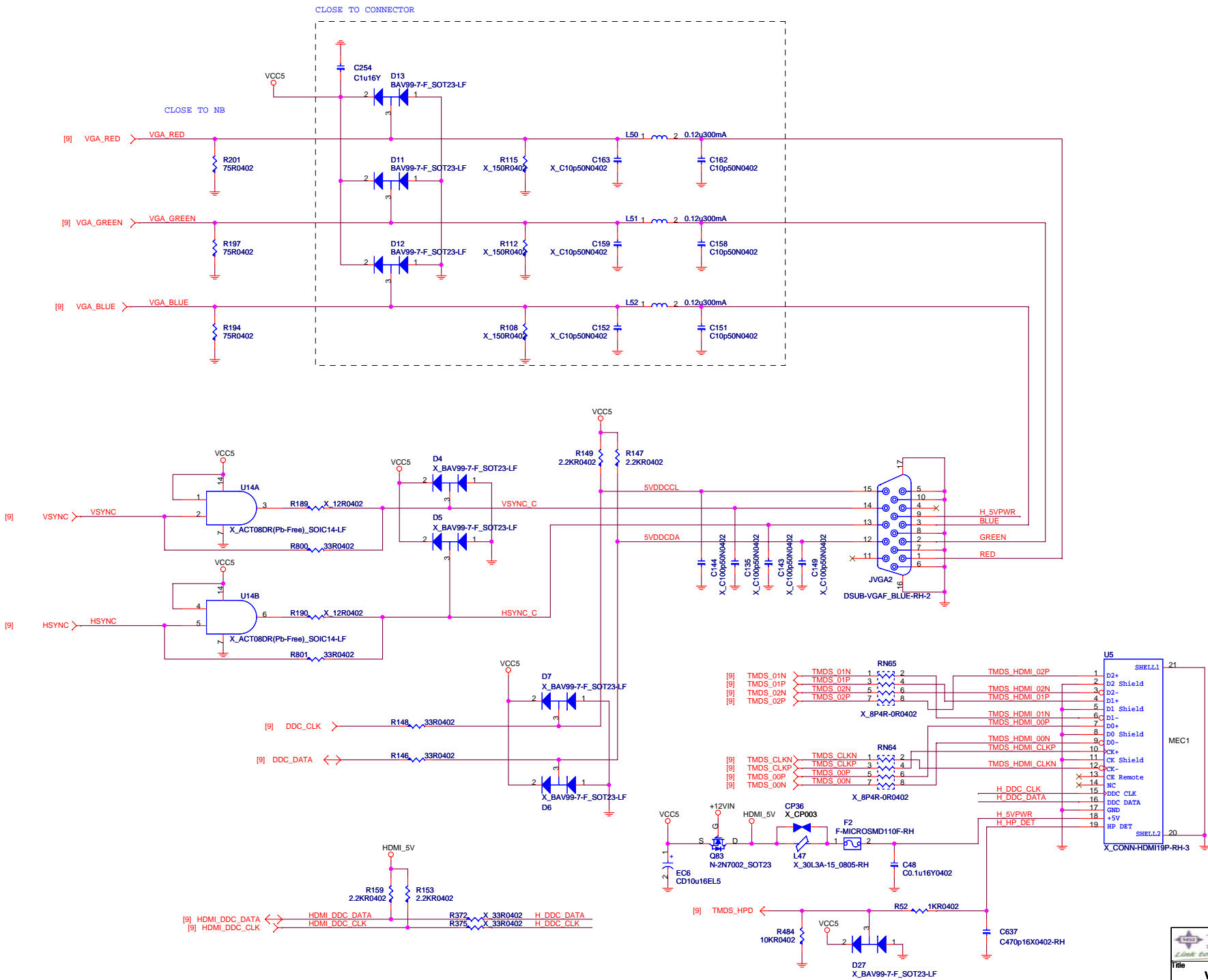
MICRO-START INT'L CO.,LTD.	
MCP73 CORE/VTT POWER	
Size	Rev
Custom	2.0
Date:	Wednesday, December 19, 2007
Sheet	14 of 36

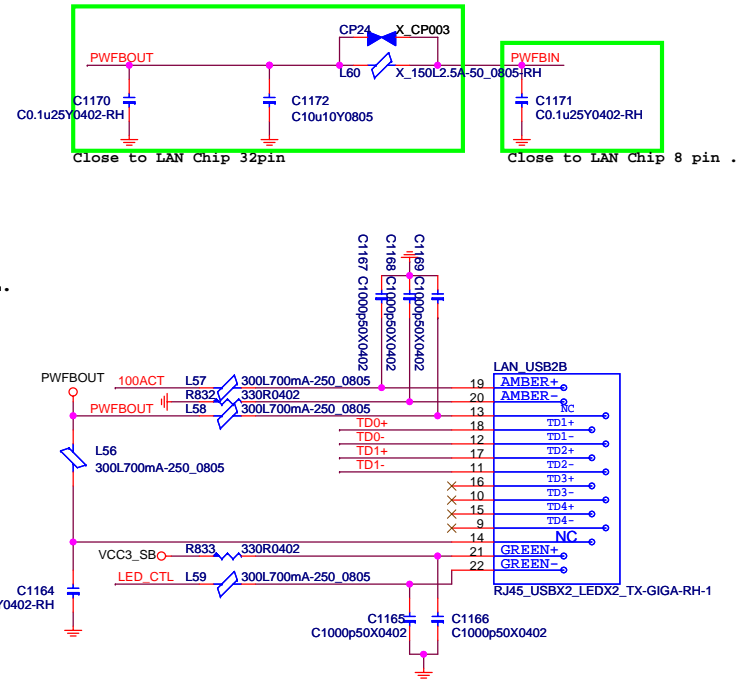
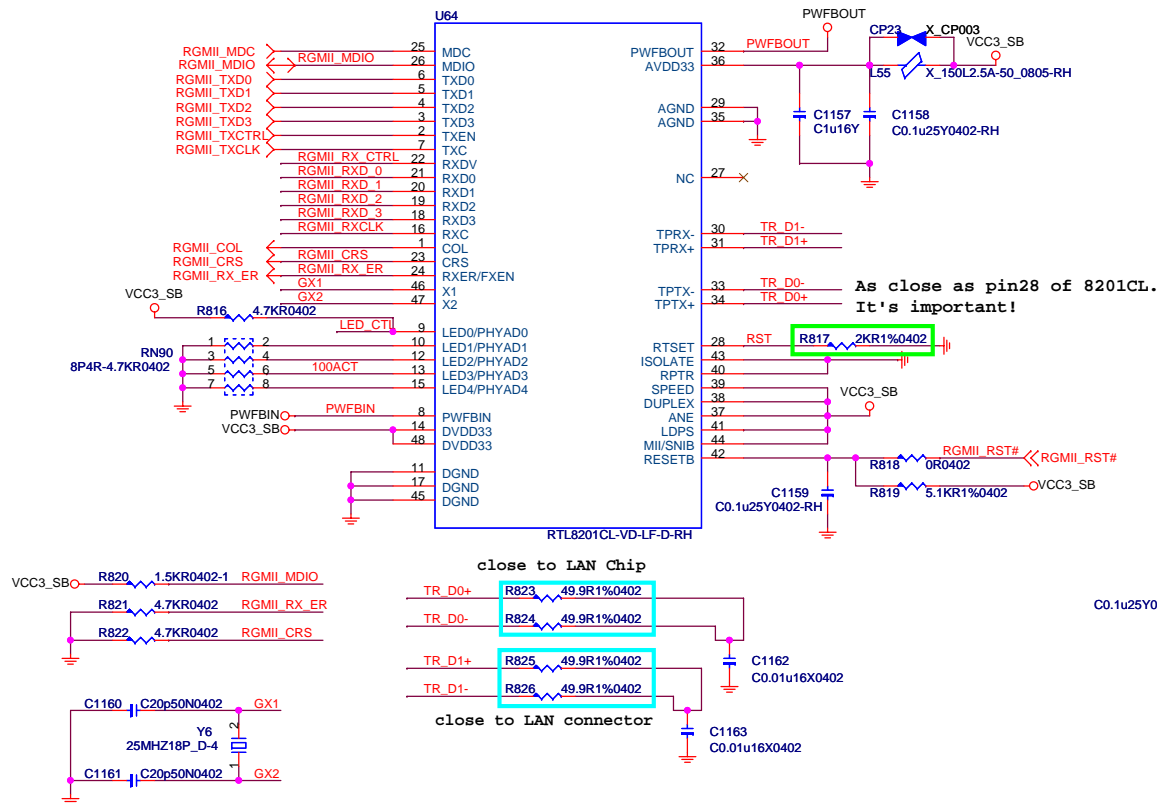
CHANNEL A VTT_DDR
DECOUPLING CAPS



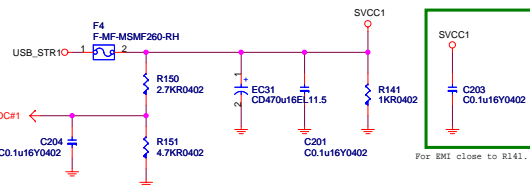
DDR II TERMINATION



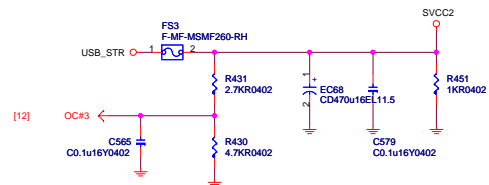




POWER CIRCUIT FOR USB PORT 0,1,2,3

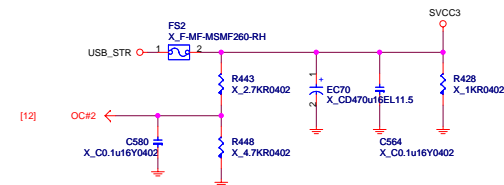


POWER CIRCUIT FOR USB PORT 4,5,6,7

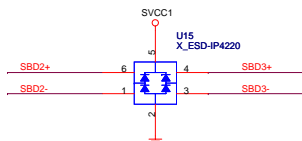
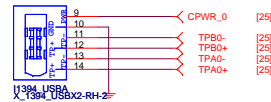
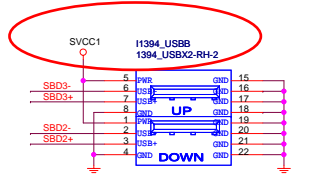
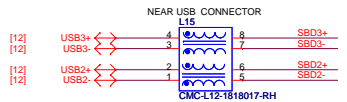


POWER CIRCUIT FOR USB PORT 8,9

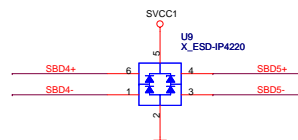
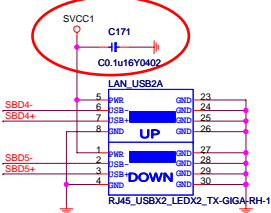
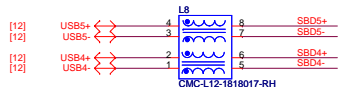
Only support 8 ports in MCP73V SKU



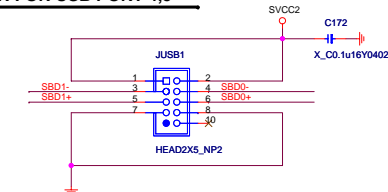
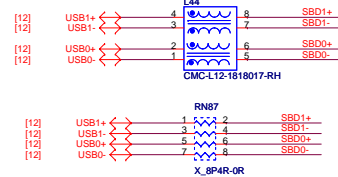
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



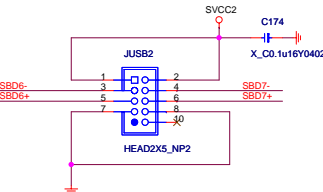
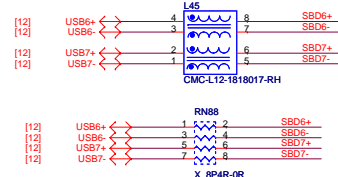
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



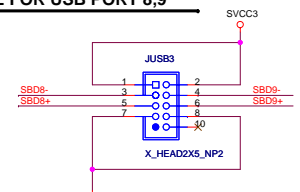
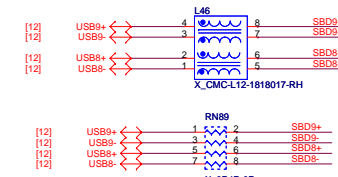
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

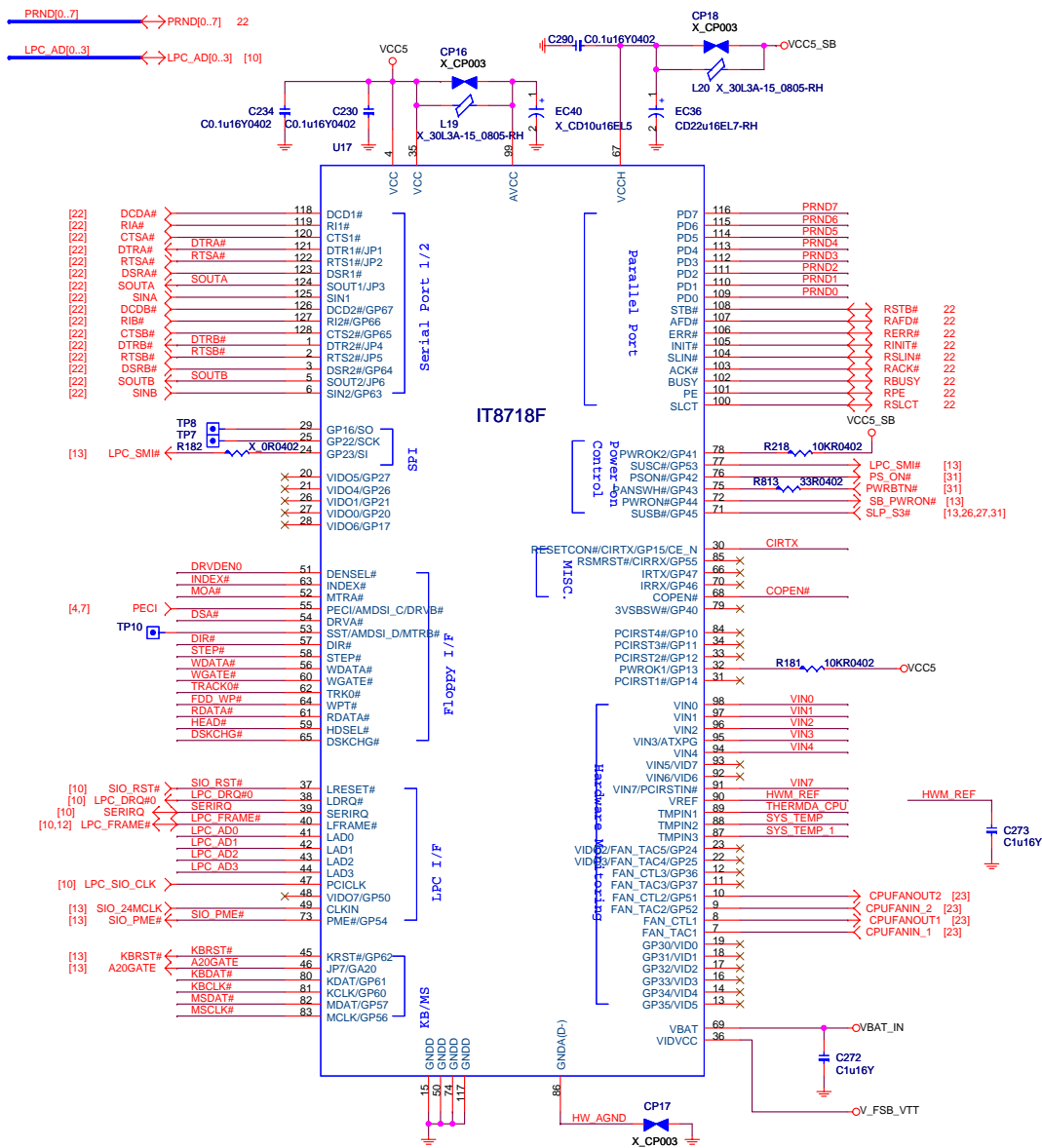


FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

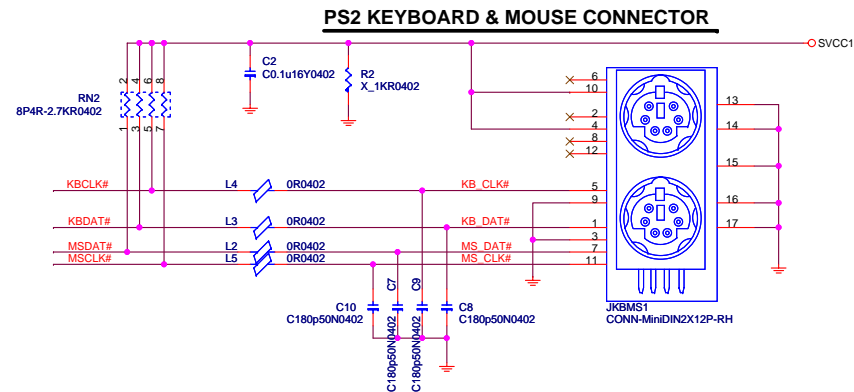


USB CARD READER + IR MODULE FOR USB PORT 8,9

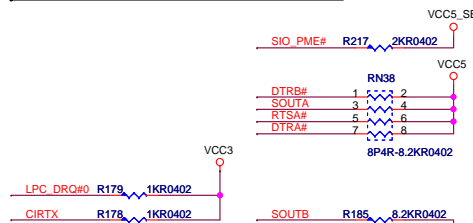




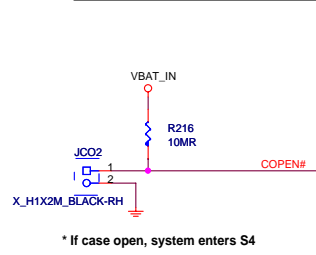
RTSB#	A20GATE	FAN DUTY
1	1	100%
1	0	75%
0	1	50%
0	0	25%



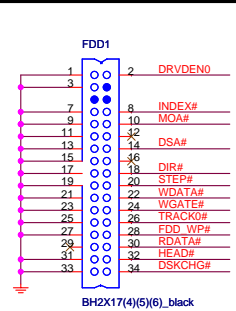
SUPER I/O STRAPPING RESISTOR



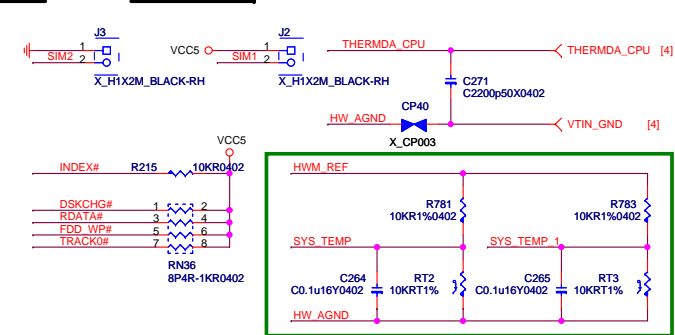
Chassis Intrusion



FLOPPY CONNECTOR

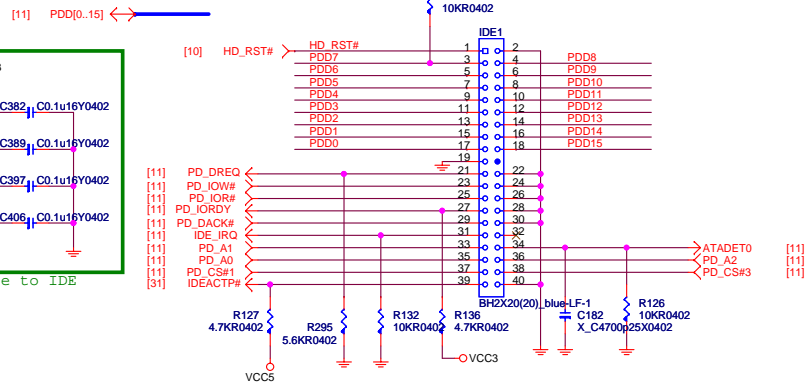


Simulation

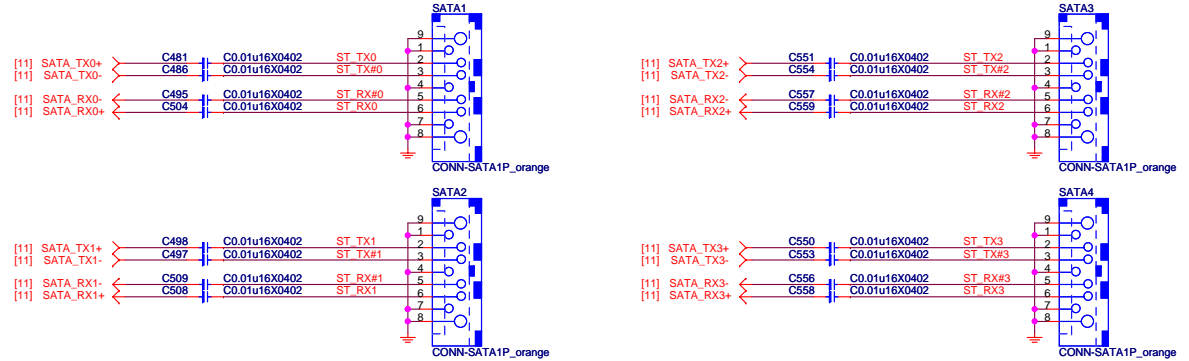


Title LPC I/O IT8718F		
Size Custom	Document Number MS-7399	Rev 2.0
Date: Friday, December 14, 2007	Sheet 21	of 36

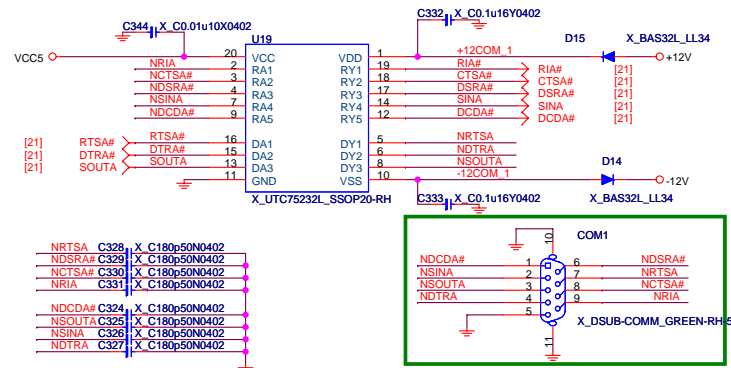
PRIMARY IDE BLOCK



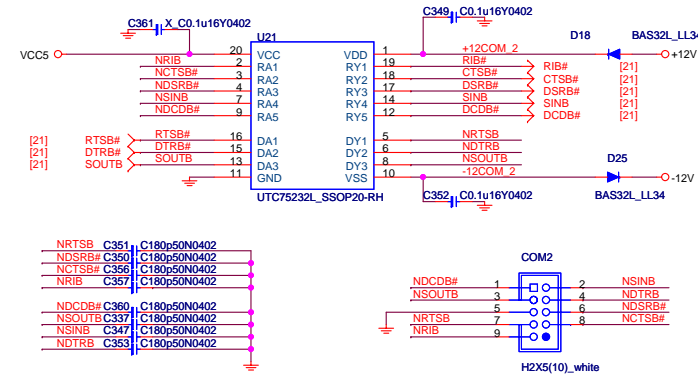
SERIAL ATA CONNECTOR BLOCK



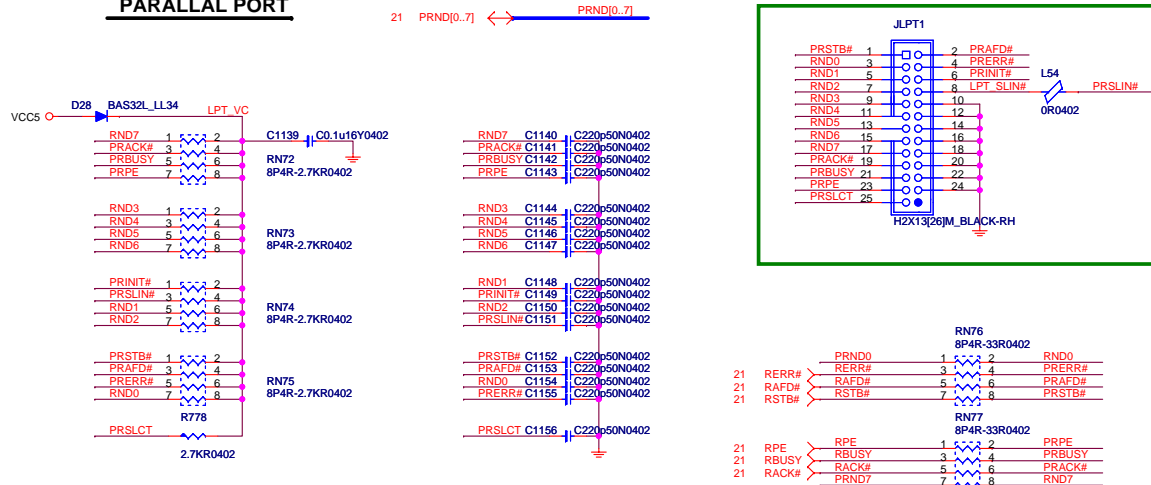
SERIAL PORT 1



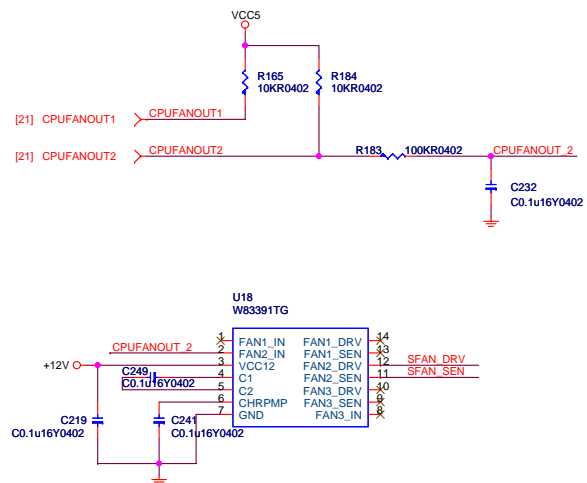
SERIAL PORT 2



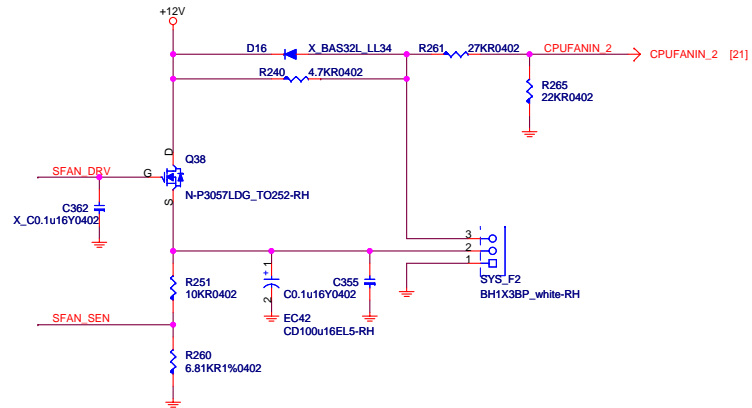
PARALLAL PORT



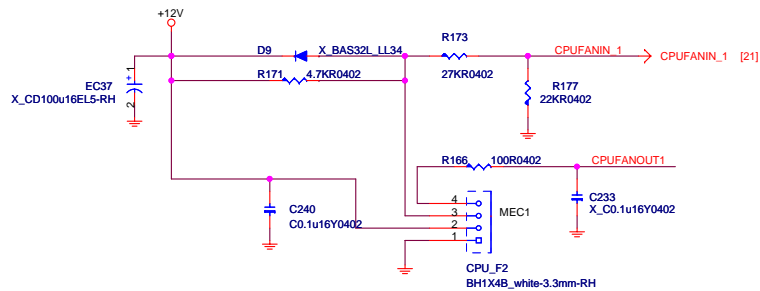
PWM FAN CONTROL



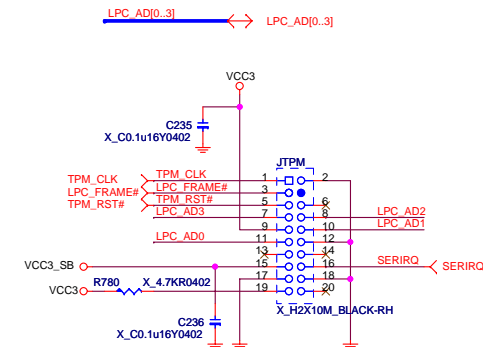
SYS FAN



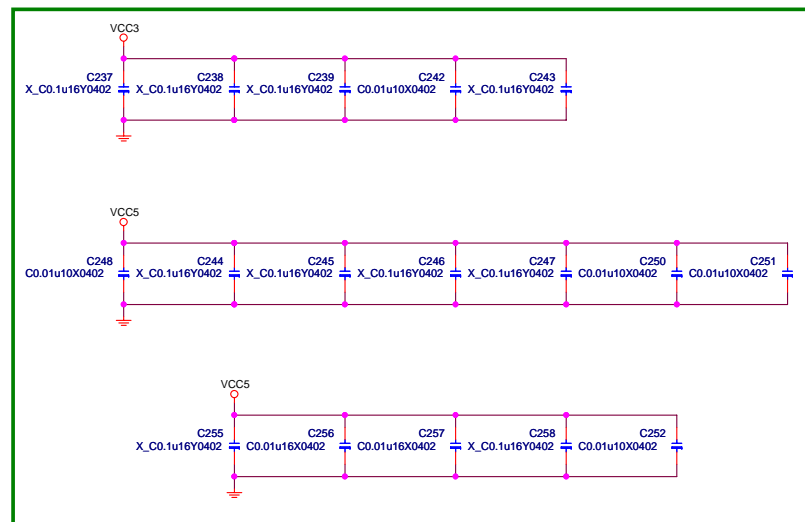
CPU FAN



TPM Header

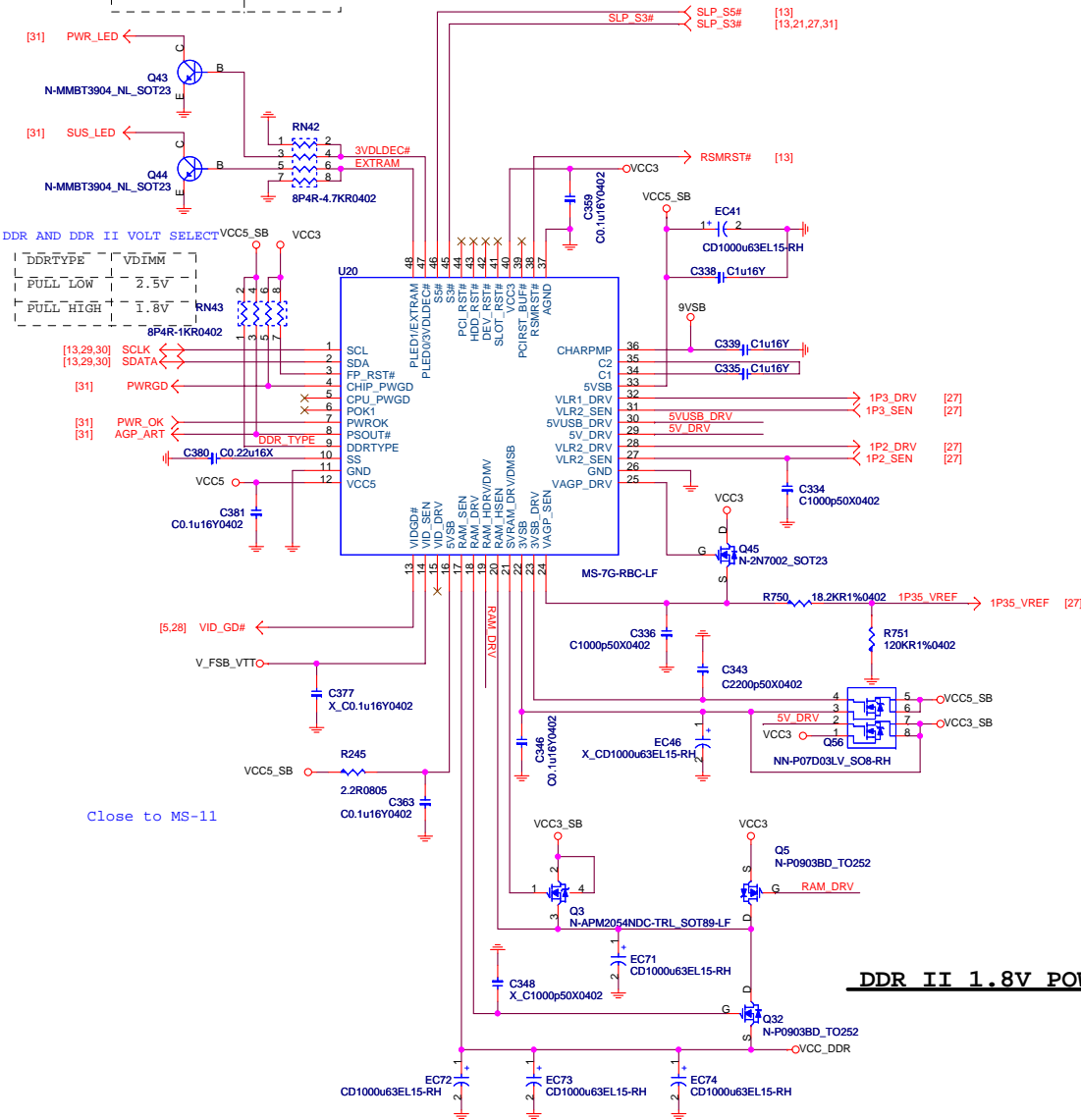


For EMI

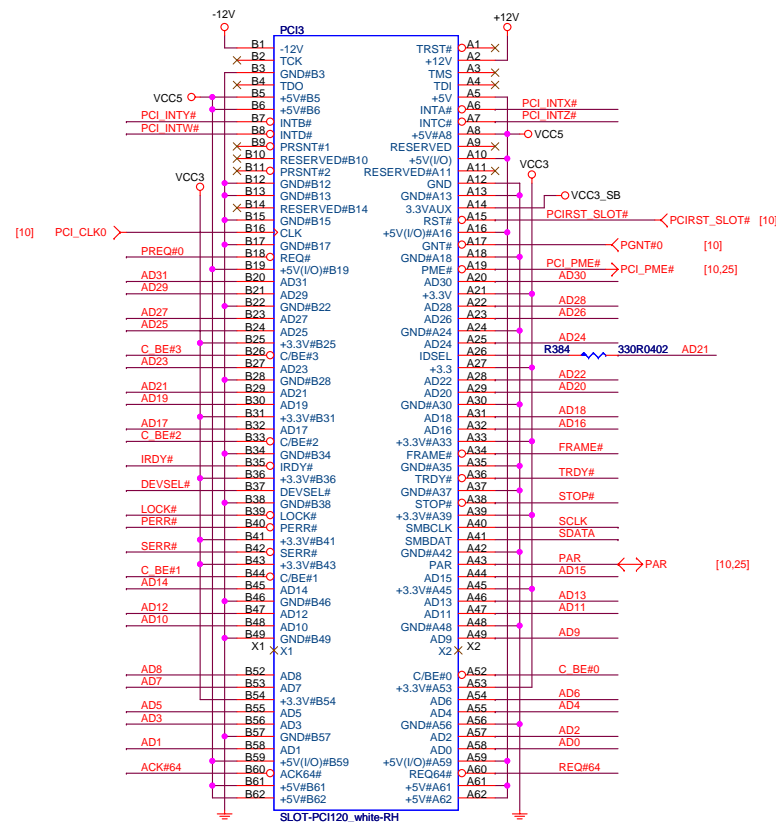


3VSB MODE SELECT	
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

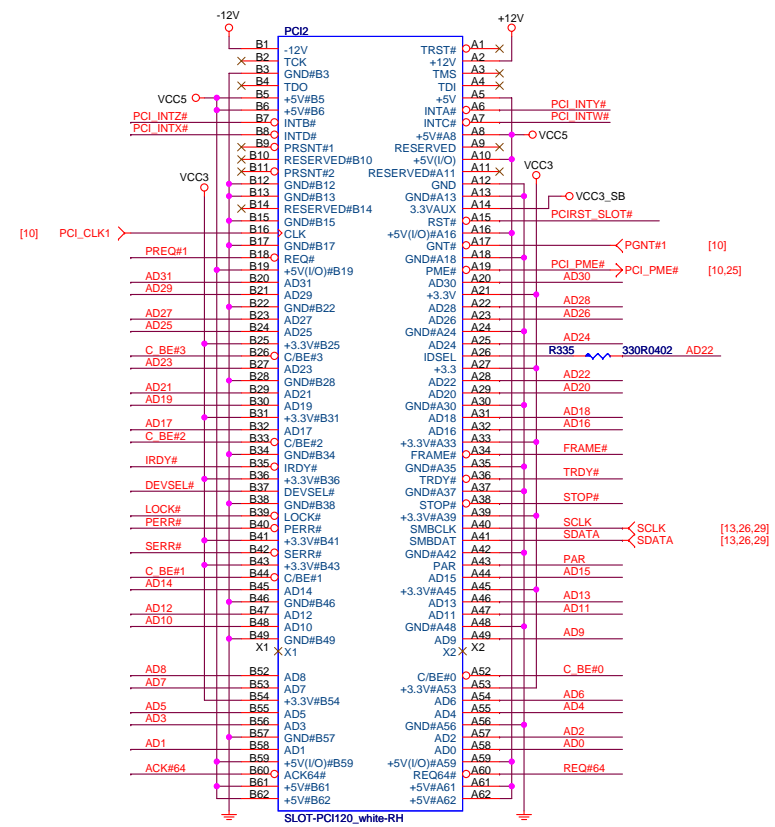


PCI SLOT 1 (PCI VER: 2.3 COMPLY)



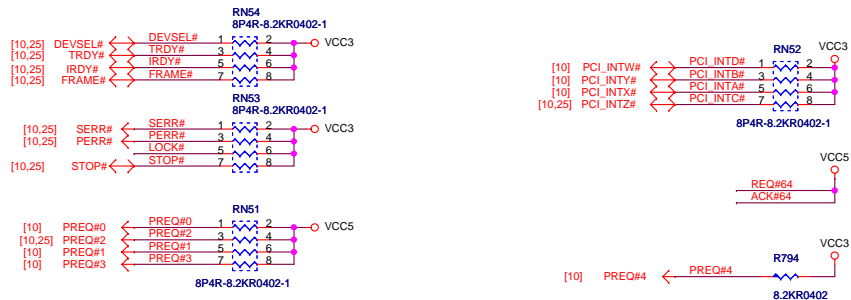
IDSEL = AD21
MASTER = PREQ#0
PCI_INTX#

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

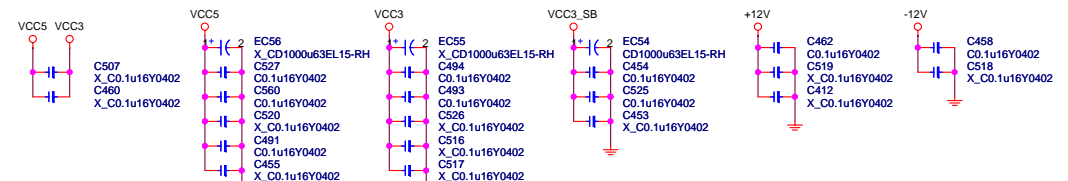


IDSEL = AD22
MASTER = PREQ#1
PCI_INTX#

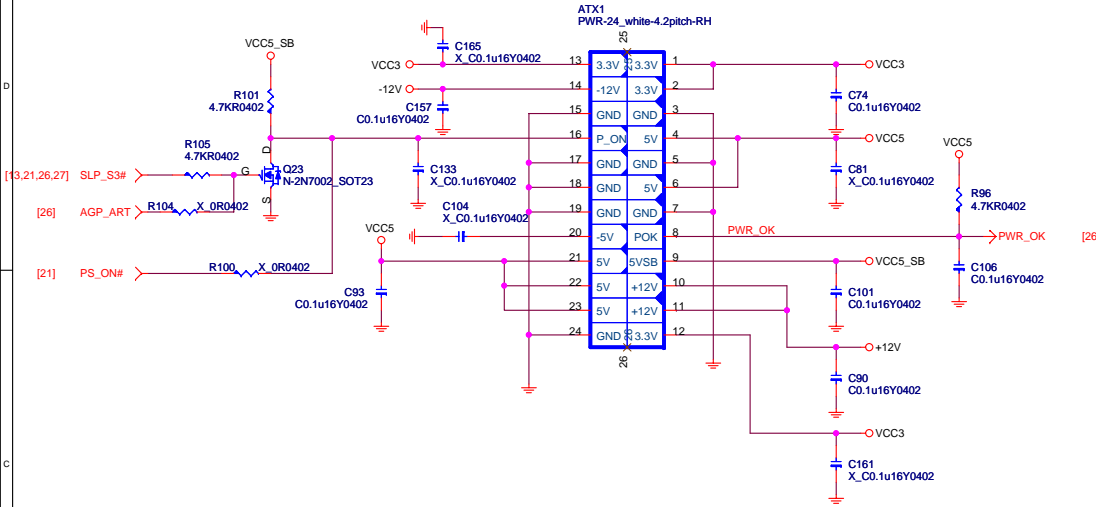
PCI PULL-UP / DOWN RESISTORS



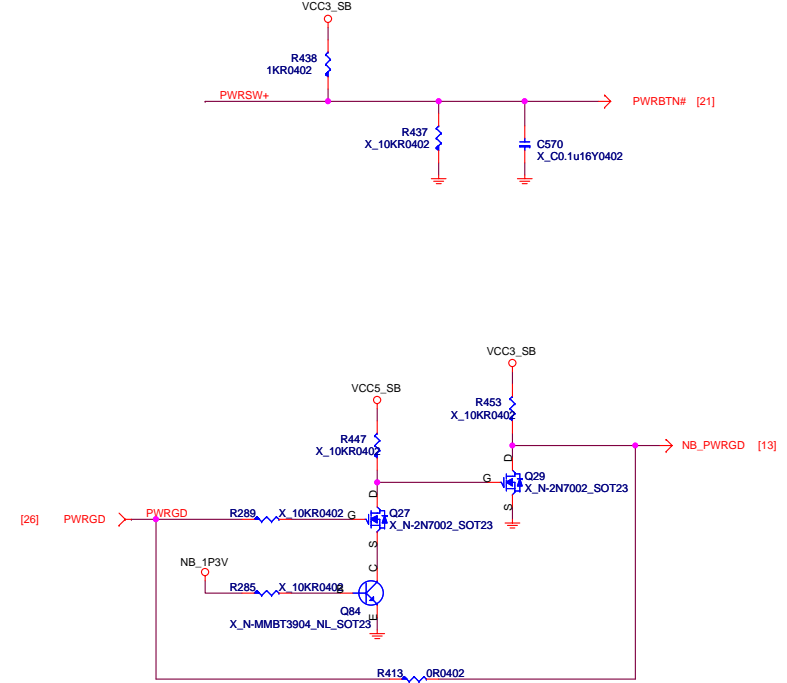
PCI SLOT DECOUPLING CAPACITORS



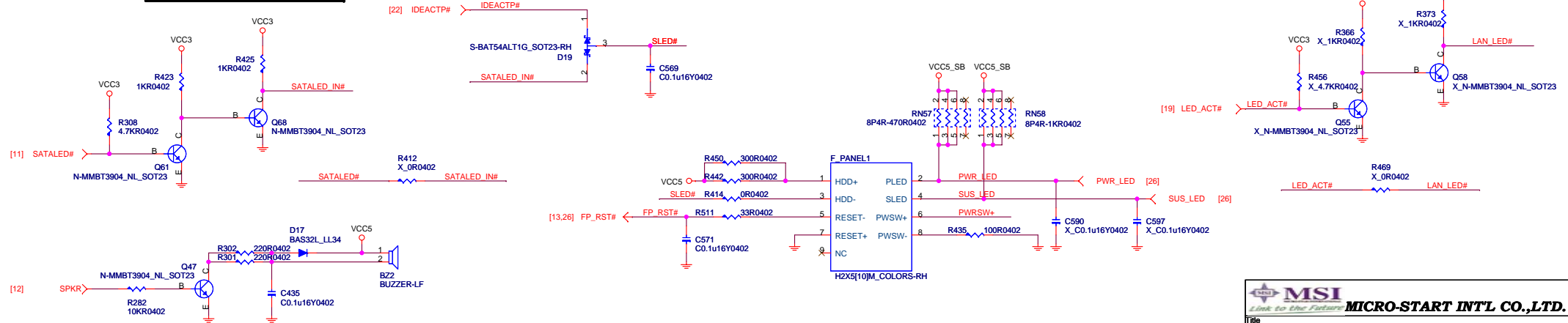
ATX CONNECTOR



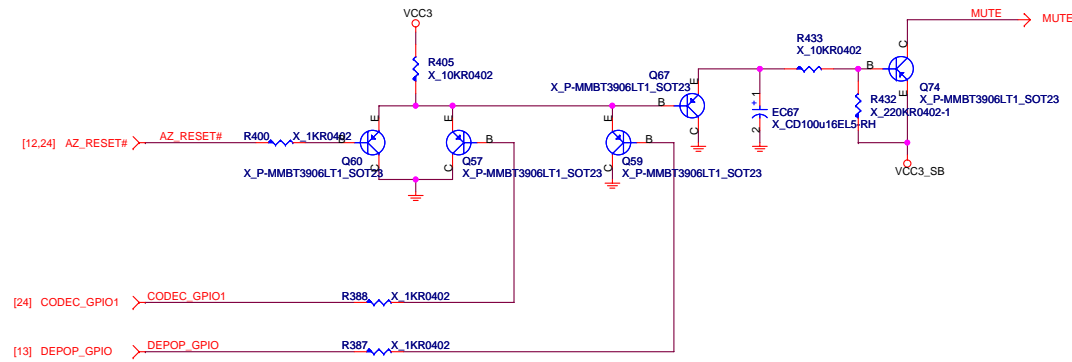
POWER BUTTON



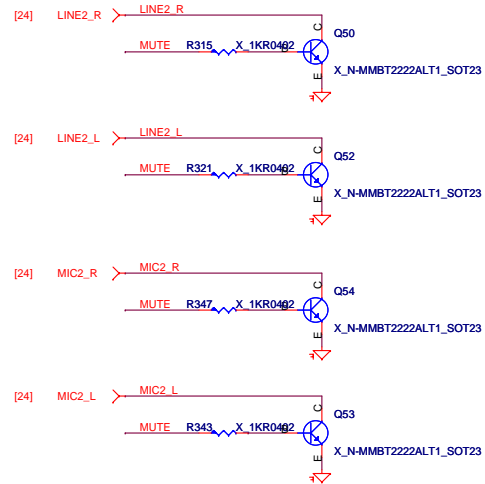
acer Front Panel Connector



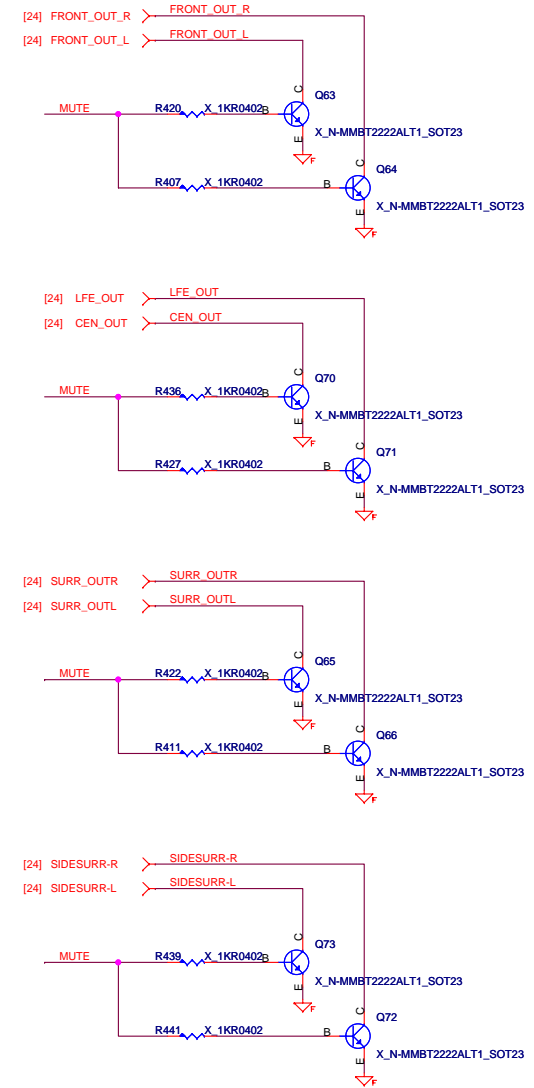
Audio De-Pop Control Circuit



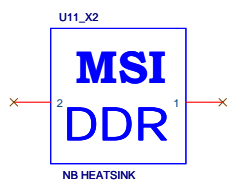
Front Audio Port De-Pop Circuit



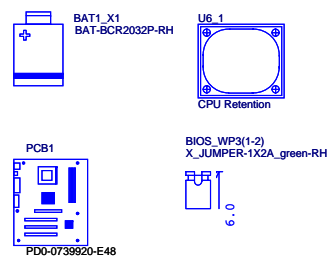
Rear Audio Port De-Pop Circuit



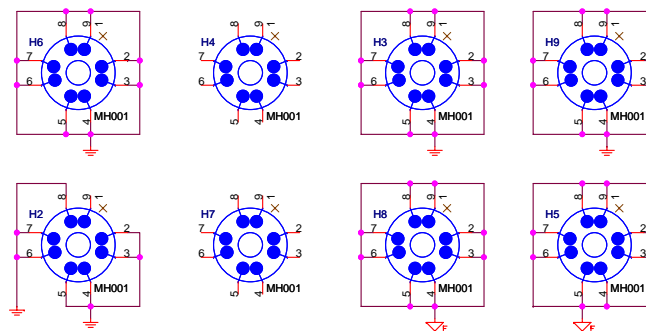
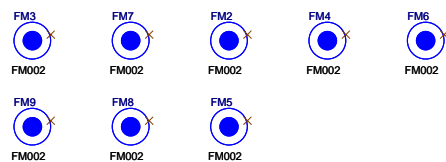
HEAT SINK

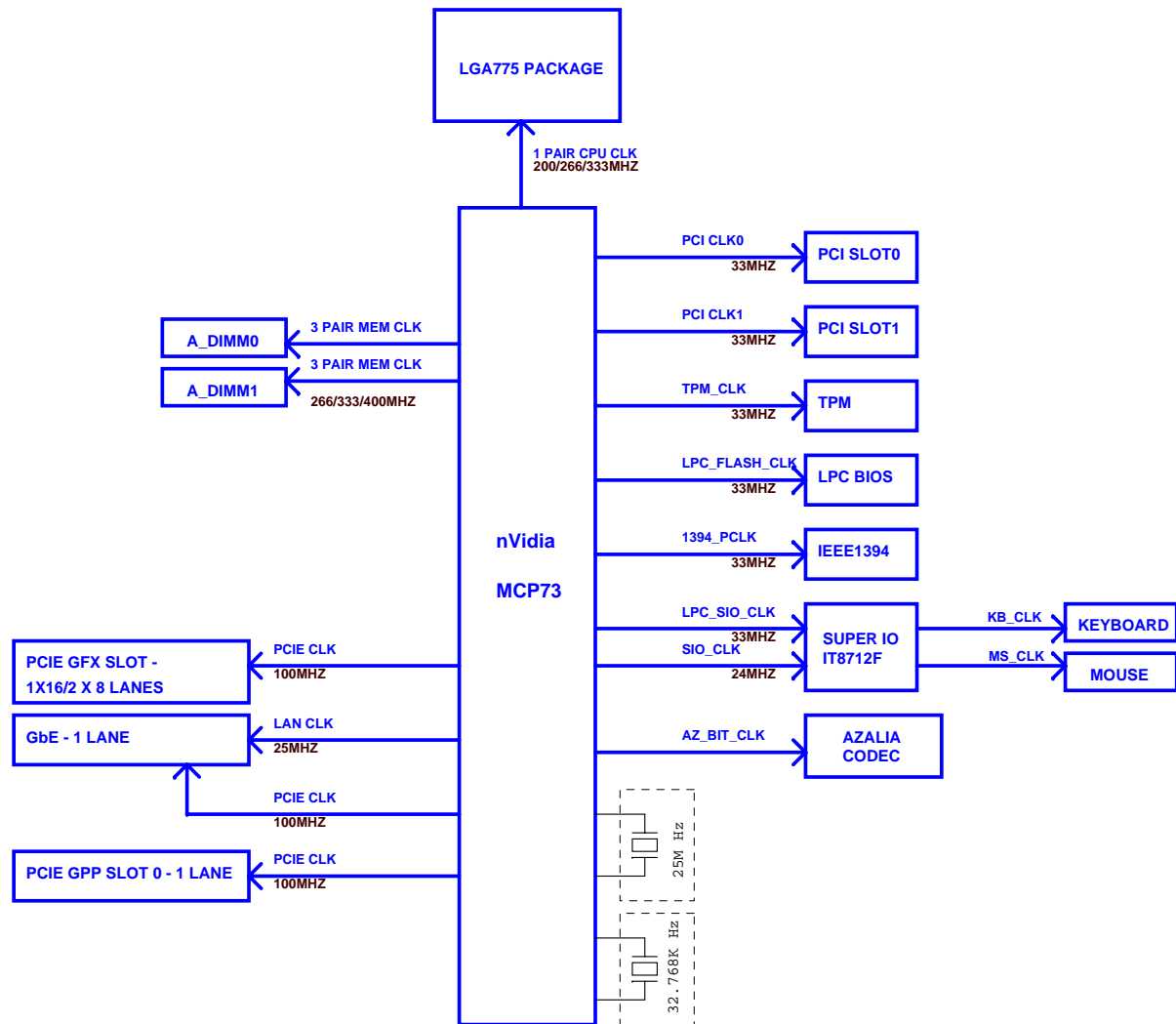


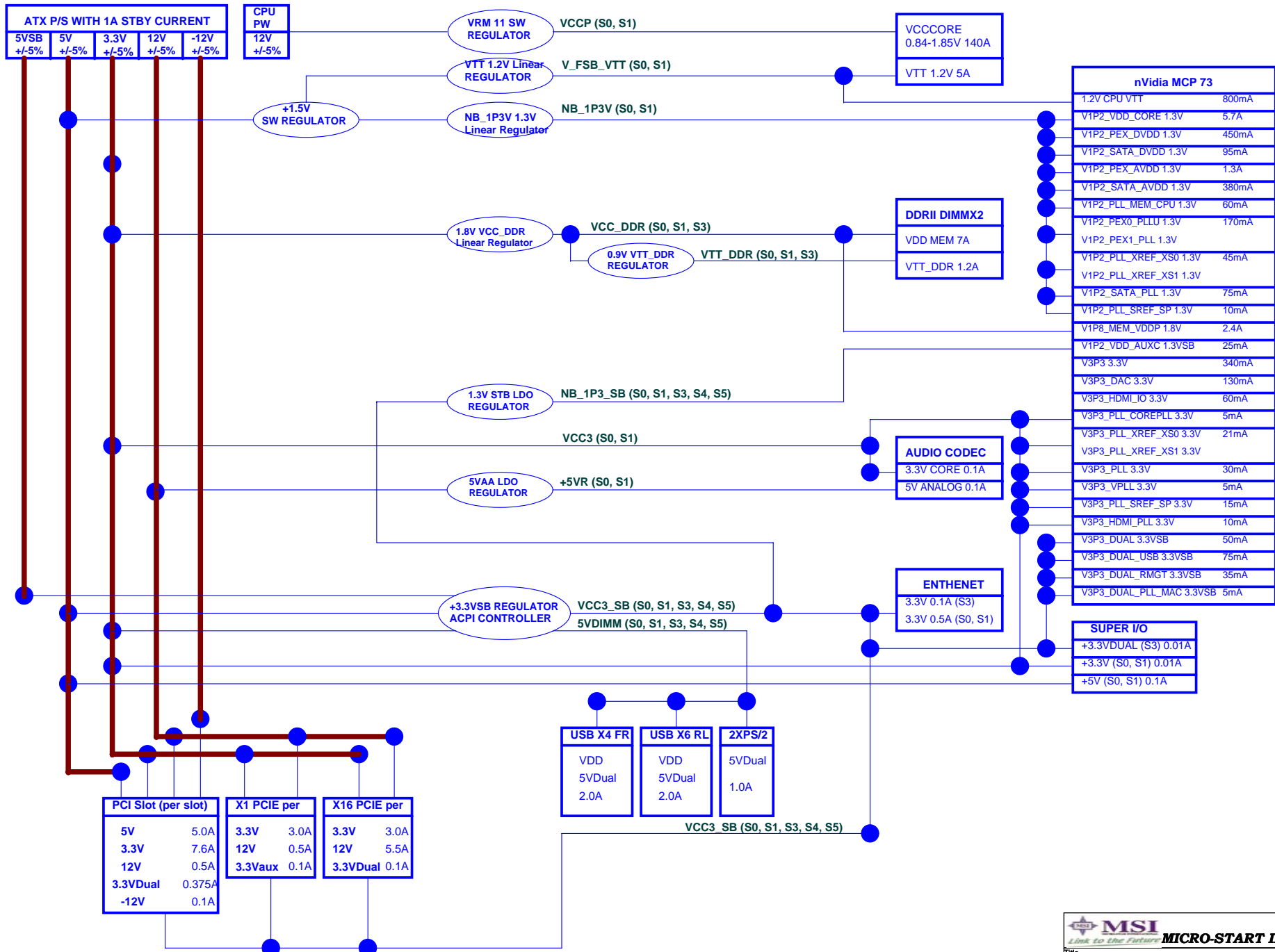
MANUAL PART

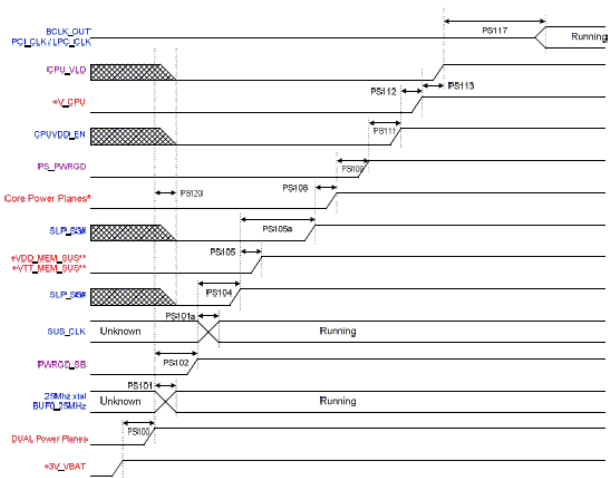


Optics Orientation Holes







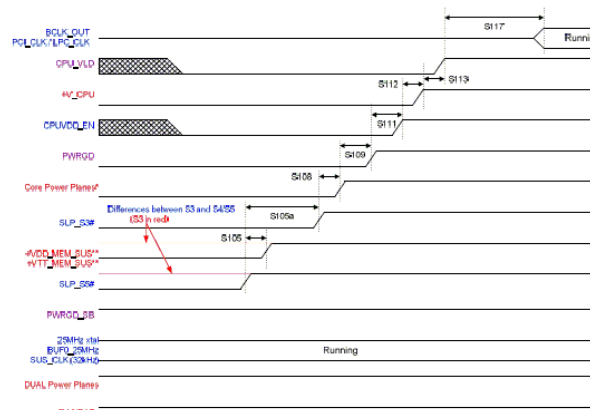


Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 G3-to-S0 Power-Up Sequence

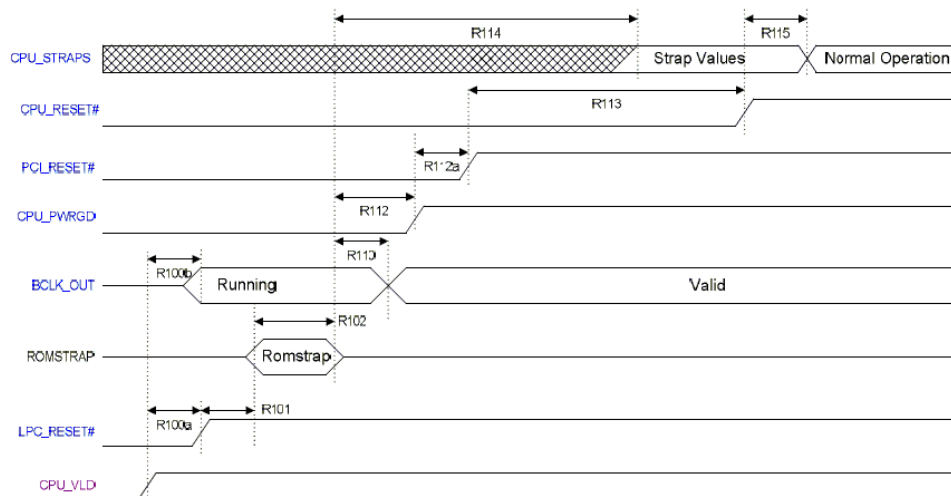


Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
- CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

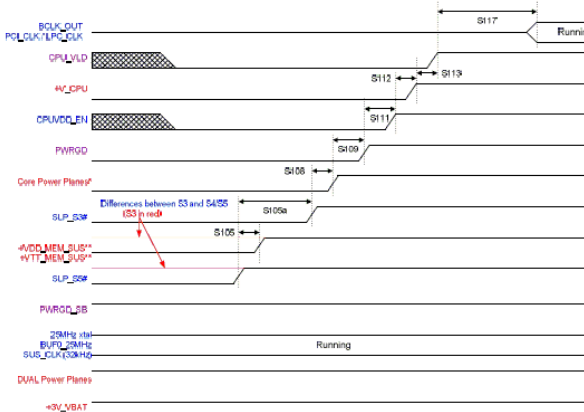
MCP73 S3/S4/S5 to S0 Power Resume Sequence



MCP73 output signals in Blue

Motherboard generated signals in Purple

MCP73 Cold Reset Power-Up Sequence



Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
- CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 S3/S4/S5 to S0 Power Resume Sequence